# 512K × 2 BANKS × 16 BITS SDRAM

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## 1. GENERAL DESCRIPTION

W9816G6IB is a high-speed synchronous dynamic random access memory (SDRAM), organized as 512K words × 2 banks × 16 bits. W9816G6IB delivers a data bandwidth of up to 166M words per second (-6). For different applications the W9816G6IB is sorted into the following speed grades: -6/-6I and -7. The -6/-6I parts can run up to 166MHz/CL3 (the -6I industrial grade which is guaranteed to support -40°C ~ 85°C). The -7 parts can run up to 143MHz/CL3.

Accesses to the SDRAM are burst oriented. Consecutive memory location in one page can be accessed at a burst length of 1, 2, 4, 8 or full page when a bank and row is selected by an ACTIVE command. Column addresses are automatically generated by the SDRAM internal counter in burst operation. Random column read is also possible by providing its address at each clock cycle. The multiple bank nature enables interleaving among internal banks to hide the precharging time.

By having a programmable Mode Register, the system can change burst length, latency cycle, interleave or sequential burst to maximize its performance. W9816G6IB is ideal for main memory in high performance applications.

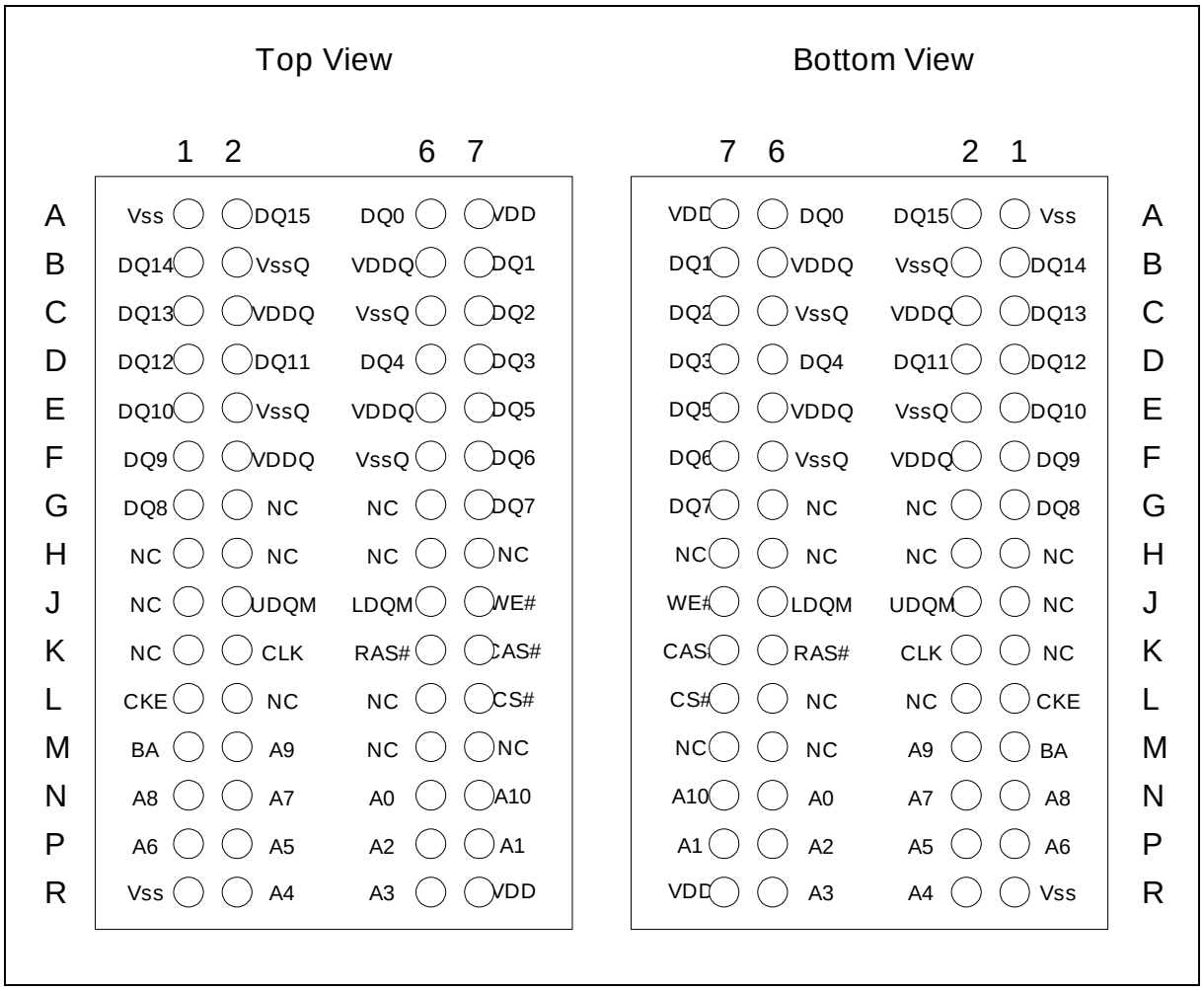
## 2. FEATURES

- 2.7V~3.6V power supply for -7 speed grade
- 3.3V ± 0.3V power supply for -6/-6I speed grade
- 524,288 words x 2 banks x 16 bits organization
- Self Refresh current: standard and low power
- CAS Latency: 2 and 3
- Burst Length: 1, 2, 4, 8 and Full Page
- Burst Read, Single Writes Mode
- Byte Data Controlled by LDQM, UDQM
- Auto-precharge and Controlled Precharge
- 4K Refresh Cycles/64 mS
- Interface: LVTTL
- Packaged in VFBGA 60 balls pitch=0.65mm, using Lead free materials with RoHS compliant

## 3. AVAILABLE PART NUMBER

| PART NUMBER | SPEED GRADE | SELF REFRESH CURRENT (MAX.) | OPERATING TEMPERATURE |
|---|---|---|---|
| W9816G6IB-6 | 166MHz/CL3 | 2mA | 0°C ~ 70°C |
| W9816G6IB-6I | 166MHz/CL3 | 2mA | -40°C ~ 85°C |
| W9816G6IB-7 | 143MHz/CL3 | 2mA | 0°C ~ 70°C |

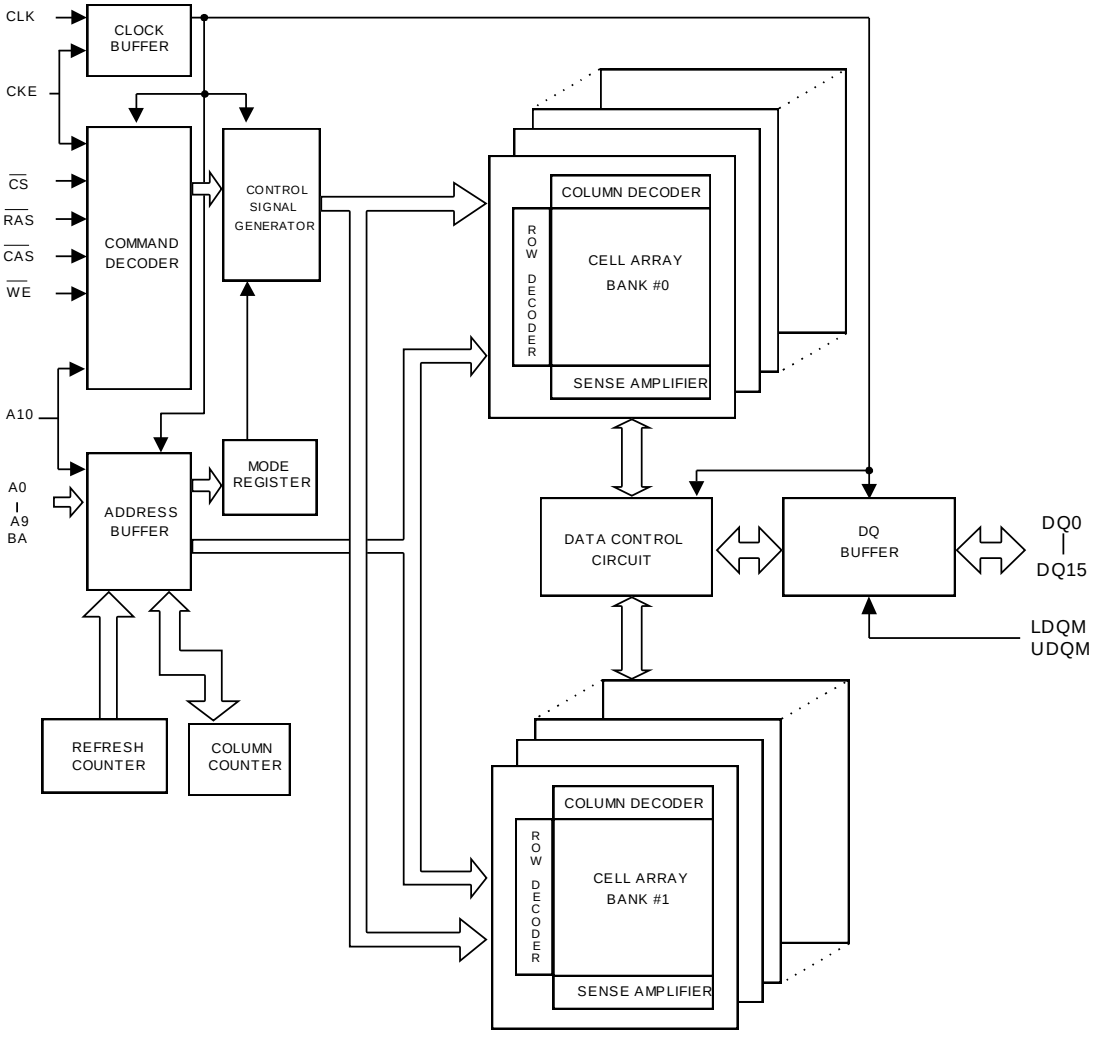
## 4. BALL CONFIGURATION



## 5. BALL DESCRIPTION

| Ball-Location | Ball Name | Function | Description |
|---|---|---|---|
| N6, P7, P6, R6, R2, P2, P1, N2, N1, M2, N7 | A0–A10 | Address | Multiplexed pins for row and column address.<br>Row address: A0–A10. Column address: A0–A7. |
| M1 | BA | Bank Address | Select bank to activate during row address latch time, or bank to read/write during column address latch time. |
| A6, B7, C7, D7, D6, E7, F7, G7, G1, F1, E1, D2, D1, C1, B1, A2, | DQ0–DQ15 | Data Input/ Output | Multiplexed pins for data input and output. |
| L7 | $\overline{CS}$ | Chip Select | Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues. |
| K6 | $\overline{RAS}$ | Row Address Strobe | Command input. When sampled at the rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed. |
| K7 | $\overline{CAS}$ | Column Address Strobe | Referred to $\overline{RAS}$ |
| J7 | $\overline{WE}$ | Write Enable | Referred to $\overline{RAS}$ |
| J2/J6 | UDQM/ LDQM | Input/Output Mask | The output buffer is placed at Hi-Z (with latency of 2) when DQM is sampled high in read cycle. In write cycle, sampling DQM high will block the write operation with zero latency. |
| K2 | CLK | Clock Inputs | System clock used to sample inputs on the rising edge of clock. |
| L1 | CKE | Clock Enable | CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode, or Self Refresh mode is entered. |
| A7, R7 | $V_{CC}$ | Power (+3.3V) | Power for input buffers and logic circuit inside DRAM. |
| A1, R1 | $V_{SS}$ | Ground | Ground for input buffers and logic circuit inside DRAM. |
| B6, C2, E6, F2 | $V_{CCQ}$ | Power (+3.3V) for I/O buffer | Separated power from $V_{CC}$, used for output buffers to improve noise immunity. |
| B2, C6, E2, F6 | $V_{SSQ}$ | Ground for I/O buffer | Separated ground from $V_{SS}$, used for output buffers to improve noise immunity. |
| G2, G6, H1, H2, H6, H7, J1, K1, L2, L6, M6, M7 | NC | No Connection | No connection. (NC pin should be connected to GND or floating) |

## 6. BLOCK DIAGRAM




Note: The cell array configuration is 2048 * 256 * 16

# 7. FUNCTIONAL DESCRIPTION

## 7.1 Power Up and Initialization

The default power up state of the mode register is unspecified. The following power up and initialization sequence need to be followed to guarantee the device being preconditioned to each user specific needs during power up, all VCC and VCCQ pins must be ramp up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power up voltage must not exceed VCC + 0.3V on any of the input pins or VCC supplies. After power up, an initial pause of 200 µS is required followed by a precharge of all banks using the precharge command. To prevent data contention on the DQ bus during power up, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. An additional eight Auto Refresh cycles (CBR) are also required before or after programming the Mode Register to ensure proper subsequent operation.

## 7.2 Programming Mode Register

After initial power up, the Mode Register Set Command must be issued for proper device operation. All banks must be in a precharged state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. The Mode Register Set Command is activated by the low signals of $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$ and $\overline{WE}$ at the positive edge of the clock. The address input data during this cycle defines the parameters to be set as shown in the Mode Register Operation table. A new command may be issued following the mode register set command once a delay equal to $t_{RSC}$ has elapsed. Please refer to the next page for Mode Register Set Cycle and Operation Table.

## 7.3 Bank Activate Command

The Bank Activate command must be applied before any Read or Write operation can be executed. The operation is similar to $\overline{RAS}$ activate in EDO DRAM. The delay from when the Bank Activate command is applied to when the first read or write operation can begin must not be less than the RAS to CAS delay time ($t_{RCD}$). Once a bank has been activated it must be precharged before another Bank Activate command can be issued to the same bank. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device ($t_{RC}$). The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank-to-Bank delay time ($t_{RRD}$). The maximum time that each bank can be held active is specified as $t_{RAS}$(max.).

## 7.4 Read and Write Access Modes

After a bank has been activated, a read or write cycle can be followed. This is accomplished by setting $\overline{RAS}$ high and $\overline{CAS}$ low at the clock rising edge after minimum of $t_{RCD}$ delay. $\overline{WE}$ pin voltage level defines whether the access cycle is a read operation ($\overline{WE}$ high), or a write operation ($\overline{WE}$ low). The address inputs determine the starting column address. Reading or writing to a different row within an activated bank requires the bank be precharged and a new Bank Activate command be issued. When more than one bank is activated, interleaved bank Read or Write operations are possible. By using the programmed burst length and alternating the access and precharge operations between multiple banks, seamless data access operation among many different pages can be realized. Read or Write Commands can also be issued to the same bank or between active banks on every clock cycle.

## 7.5 Burst Read Command

The Burst Read command is initiated by applying logic low level to $\overline{CS}$ and $\overline{CAS}$ while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The Mode Register sets type of burst (sequential or interleave) and the burst length (1, 2, 4, 8 and full page) during the Mode Register Set Up cycle. Table 2 and 3 in the next page explain the address sequence of interleave mode and sequence mode.

## 7.6 Burst Write Command

The Burst Write command is initiated by applying logic low level to $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. Data for the first burst write cycle must be applied on the DQ pins on the same clock cycle that the Write Command is issued. The remaining data inputs must be supplied on each subsequent rising clock edge until the burst length is completed. Data supplied to the DQ pins after burst finishes will be ignored.

## 7.7 Read Interrupted by a Read

A Burst Read may be interrupted by another Read Command. When the previous burst is interrupted, the remaining addresses are overridden by the new read address with the full burst length. The data from the first Read Command continues to appear on the outputs until the CAS Latency from the interrupting Read Command the is satisfied.

## 7.8 Read Interrupted by a Write

To interrupt a burst read with a Write Command, DQM may be needed to place the DQs (output drivers) in a high impedance state to avoid data contention on the DQ bus. If a Read Command will issue data on the first and second clocks cycles of the write operation, DQM is needed to insure the DQs are tri-stated. After that point the Write Command will have control of the DQ bus and DQM masking is no longer needed.

## 7.9 Write Interrupted by a Write

A burst write may be interrupted before completion of the burst by another Write Command. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

## 7.10 Write Interrupted by a Read

A Read Command will interrupt a burst write operation on the same clock cycle that the Read Command is activated. The DQs must be in the high impedance state at least one cycle before the new read data appears on the outputs to avoid data contention. When the Read Command is activated, any residual data from the burst write cycle will be ignored.

## 7.11 Burst Stop Command

A Burst Stop Command may be used to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank, if the burst length is full page. Use of the Burst Stop Command during other burst length operations is illegal. The Burst Stop Command is defined by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock. The data DQs go to a high impedance state after a delay, which is equal to the $\overline{CAS}$ Latency in a burst read cycle, interrupted by Burst Stop. If a Burst Stop Command is issued during a full page burst write operation, then any residual data from the burst write cycle will be ignored.

## 7.12 Addressing Sequence of Sequential Mode

A column access is performed by increasing the address from the column address, which is input to the device. The disturb address is varied by the Burst Length as shown in Table 2.

**Table 2 Address Sequence of Sequential Mode**

| DATA | ACCESS ADDRESS | BURST LENGTH |
|---|---|---|
| Data 0 | n | BL = 2 (disturb address is A0) |
| Data 1 | n + 1 | No address carry from A0 to A1 |
| Data 2 | n + 2 | BL = 4 (disturb addresses are A0 and A1) |
| Data 3 | n + 3 | No address carry from A1 to A2 |
| Data 4 | n + 4 | |
| Data 5 | n + 5 | BL = 8 (disturb addresses are A0, A1 and A2) |
| Data 6 | n + 6 | No address carry from A2 to A3 |
| Data 7 | n + 7 | |

## 7.13 Addressing Sequence of Interleave Mode

A column access is started in the input column address and is performed by inverting the address bit in the sequence shown in Table 3.

**Table 3 Address Sequence of Interleave Mode**

| DATA | ACCESS ADDRESS | BURST LENGTH |
|---|---|---|
| Data 0 | A8 A7 A6 A5 A4 A3 A2 A1 A0 | BL = 2 |
| Data 1 | A8 A7 A6 A5 A4 A3 A2 A1 $\overline{A0}$ | |
| Data 2 | A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ A0 | BL = 4 |
| Data 3 | A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ $\overline{A0}$ | |
| Data 4 | A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 A0 | BL = 8 |
| Data 5 | A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 $\overline{A0}$ | |
| Data 6 | A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ A0 | |
| Data 7 | A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ $\overline{A0}$ | |

## 7.14 Auto-precharge Command

If A10 is set to high when the Read or Write Command is issued, then the Auto-precharge function is entered. During Auto-precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge automatically before all burst read cycles have been completed. Regardless of burst length, it will begin a certain number of clocks prior to the end of the scheduled burst cycle. The number of clocks is determined by CAS Latency.

A Read or Write Command with Auto-precharge can not be interrupted before the entire burst operation is completed. Therefore, use of a Read, Write, or Precharge Command is prohibited during a read or write cycle with Auto-precharge. Once the precharge operation has started, the bank cannot be reactivated until the Precharge time ($t_{RP}$) has been satisfied. Issue of Auto-precharge command is illegal if the burst is set to full page length. If A10 is high when a Write Command is issued, the Write with Auto-precharge function is initiated. The SDRAM automatically enters the precharge operation two clock delay from the last burst write cycle. This delay is referred to as Write $t_{WR}$. The bank undergoing Auto-precharge can not be reactivated until $t_{WR}$ and $t_{RP}$ are satisfied. This is referred to as $t_{DAL}$, Data-in to Active delay ($t_{DAL}$ = $t_{WR}$ + $t_{RP}$). When using the Auto-precharge Command, the interval between the Bank Activate Command and the beginning of the internal precharge operation must satisfy $t_{RAS}$(min).

## 7.15 Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is entered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank separately or all banks simultaneously. The address bits, A10, and BA, are used to define which bank(s) is to be precharged when the command is issued. After the Precharge Command is issued, the precharged bank must be reactivated before a new read or write access can be executed. The delay between the Precharge Command and the Activate Command must be greater than or equal to the Precharge time ($t_{RP}$).

## 7.16 Self Refresh Command

The Self-Refresh Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. All banks must be idle prior to issuing the Self-Refresh Command. Once the command is registered, CKE must be held low to keep the device in Self-Refresh mode. When the SDRAM has entered Self Refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self-Refresh Operation to save power. The device will exit Self-Refresh operation after CKE is returned high. Any subsequent commands can be issued after $t_{XSR}$ from the end of Self Refresh command.

If, during normal operation, Auto-Refresh cycles are issued in bursts (as opposed to being evenly distributed), a burst of 2,048 Auto-Refresh cycles should be completed just prior to entering and just after exiting the Self-Refresh mode.

## 7.17 Power Down Mode

The Power Down mode is initiated by holding CKE low. All of the receiver circuits except CKE are gated off to reduce the power. The Power Down mode does not perform any refresh operations; therefore the device can not remain in Power Down mode longer than the Refresh period ($t_{REF}$) of the device.

The Power Down mode is exited by bringing CKE high. When CKE goes high, a No Operation Command is required on the next rising clock edge, depending on $t_{CK}$. The input buffers need to be enabled with CKE held high for a period equal to $t_{CKS}$(min) + $t_{CK}$(min).

## 7.18 No Operation Command

The No Operation Command should be used in cases when the SDRAM is in an idle or a wait state to prevent the SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

## 7.19 Deselect Command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when $\overline{CS}$ is brought high, the $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ signals become don't cares.

## 7.20 Clock Suspend Mode

During normal access mode, CKE must be held high enabling the clock. When CKE is registered low while at least one of the banks is active, Clock Suspend Mode is entered. The Clock Suspend mode deactivates the internal clock and suspends any clocked operation that was currently being executed. There is a one-clock delay between the registration of CKE low and the time at which the SDRAM operation suspends. While in Clock Suspend mode, the SDRAM ignores any new commands that are issued. The Clock Suspend mode is exited by bringing CKE high. There is a one-clock cycle delay from when CKE returns high to when Clock Suspend mode is exited.

## 8. OPERATION MODE

Fully synchronous operations are performed to latch the commands at the positive edges of CLK. Table 1 shows the truth table for the operation commands.

**TABLE 1 TRUTH TABLE (NOTE 1, 2)**

| COMMAND | DEVICE STATE | CKEn-1 | CKEn | DQM | BA | A10 | A9-A0 | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Bank Active | Idle | H | X | X | V | V | V | L | L | H | H |
| Bank Precharge | Any | H | X | X | V | L | X | L | L | H | L |
| Precharge All | Any | H | X | X | X | H | X | L | L | H | L |
| Write | Active (3) | H | X | X | V | L | V | L | H | L | L |
| Write with Auto-precharge | Active (3) | H | X | X | V | H | V | L | H | L | L |
| Read | Active (3) | H | X | X | V | L | V | L | H | L | H |
| Read with Auto-precharge | Active (3) | H | X | X | V | H | V | L | H | L | H |
| Mode Register Set | Idle | H | X | X | V | V | V | L | L | L | L |
| No-Operation | Any | H | X | X | X | X | X | L | H | H | H |
| Burst Stop | Active (4) | H | X | X | X | X | X | L | H | H | L |
| Device Deselect | Any | H | X | X | X | X | X | H | X | X | X |
| Auto-Refresh | Idle | H | H | X | X | X | X | L | L | L | H |
| Self-Refresh Entry | Idle | H | L | X | X | X | X | L | L | L | H |
| Self-Refresh Exit | Idle<br>(S.R) | L<br>L | H<br>H | X<br>X | X<br>X | X<br>X | X<br>X | H<br>L | X<br>H | X<br>H | X<br>X |
| Clock Suspend Mode Entry | Active | H | L | X | X | X | X | X | X | X | X |
| Power Down Mode Entry | Idle<br>Active (5) | H<br>H | L<br>L | X<br>X | X<br>X | X<br>X | X<br>X | H<br>L | X<br>H | X<br>H | X<br>X |
| Clock Suspend Mode Exit | Active | L | H | X | X | X | X | X | X | X | X |
| Power Down Mode Exit | Any<br>(power down) | L<br>L | H<br>H | X<br>X | X<br>X | X<br>X | X<br>X | H<br>L | X<br>H | X<br>H | X<br>X |
| Data Write/Output Enable | Active | H | X | L | X | X | X | X | X | X | X |
| Data Write/Output Disable | Active | H | X | H | X | X | X | X | X | X | X |

**Notes :**(1) V = Valid, X = Don't care, L = Low Level, H = High Level

(2) CKEn signal is input level when commands are provided.
CKEn-1 signal is the input level one clock cycle before the command is issued.

(3) These are state of bank designated by BA signals.

(4) Device state is full page burst operation.

(5) Power Down Mode can not be entered in the burst cycle.
When this command asserts in the burst cycle, device state is clock suspend mode.

# 9. ELECTRICAL CHARACTERISTICS

## 9.1 Absolute Maximum Ratings

| PARAMETER | SYMBOL | RATING | UNIT | NOTES |
|---|---|---|---|---|
| Input, Output Voltage | $V_{IN}$, $V_{OUT}$ | -1 ~ $V_{CC}$ + 0.3 | V | 1 |
| Power Supply Voltage | $V_{CC}$, $V_{CCQ}$ | -1~ 4.6 | V | 1 |
| Operating Temperature for -6/-7 | $T_{OPR}$ | 0 ~ 70 | °C | 1 |
| Operating Temperature for -6I | $T_{OPR}$ | -40 ~ 85 | °C | 1 |
| Storage Temperature | $T_{STG}$ | -55 ~ 150 | °C | 1 |
| Soldering Temperature (10s) | $T_{SOLDER}$ | 260 | °C | 1 |
| Power Dissipation | $P_D$ | 1 | W | 1 |
| Short Circuit Output Current | $I_{OUT}$ | 50 | mA | 1 |

**Note:** Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

## 9.2 Recommended DC Operating Conditions

($T_A$ = 0 to 70°C for -6/-7 , $T_A$= -40 to 85°C for -6I)

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | NOTES |
|---|---|---|---|---|---|---|
| Power Supply Voltage for -6/-6I | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V | 2 |
| Power Supply Voltage for -7 | $V_{CC}$ | 2.7 | 3.3 | 3.6 | V | 2 |
| Power Supply Voltage for -6/-6I (for I/O Buffer) | $V_{CCQ}$ | 3.0 | 3.3 | 3.6 | V | 2 |
| Power Supply Voltage for -7 (for I/O Buffer) | $V_{CCQ}$ | 2.7 | 3.3 | 3.6 | V | 2 |
| Input High Voltage | $V_{IH}$ | 2.0 | - | $V_{CC}$ + 0.3 | V | 2 |
| Input Low Voltage | $V_{IL}$ | -0.3 | - | 0.8 | V | 2 |

**Note:** $V_{IH}$ (max.) = $V_{CC}$/$V_{CCQ}$ +1.5V for pulse width ≤ 5 nS

$V_{IL}$ (min.) = $V_{SS}$/$V_{SSQ}$ -1.5V for pulse width ≤ 5 nS

## 9.3 Capacitance

($V_{CC}$ = 3.3V ±0.3V, $T_A$ = 25 °C, f = 1MHz)

| PARAMETER | SYM. | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Input Capacitance (A0 to A10, BA, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, UDQM, LDQM, CKE) | $C_I$ | - | 4 | pf |
| Input Capacitance (CLK) | | - | 4 | pf |
| Input/Output capacitance (DQ0 to DQ15) | $C_{IO}$ | - | 5.5 | pf |

**Note:** These parameters are periodically sampled and not 100% tested

## 9.4 DC Characteristics

($V_{CC}$ = 3.3V ±0.3V for -6/-6I, $V_{CC}$ = 2.7V to 3.6V for -7, $T_A$ = 0 to 70°C for -6/-7, $T_A$= -40 to 85°C for -6I)

| PARAMETER | | SYM. | MAX. | | UNIT | NOTES |
|---|---|---|---|---|---|---|
| | | | -6/-6I | -7 | | |
| Operating Current<br>$t_{CK}$ = min., $t_{RC}$ = min.<br>Active precharge command cycling without burst operation | 1 Bank Operation | $I_{CC1}$ | 60 | 50 | mA | 3 |
| Standby Current<br>$t_{CK}$ = min., $\overline{CS}$ = $V_{IH}$<br>$V_{IH/L}$ = $V_{IH}$ (min.) / $V_{IL}$ (max.)<br>Bank: inactive state | CKE = $V_{IH}$ | $I_{CC2}$ | 30 | 25 | | 3 |
| | CKE = $V_{IL}$<br>(Power Down mode) | $I_{CC2P}$ | 2 | 2 | | 3 |
| Standby Current<br>CLK = $V_{IL}$, $\overline{CS}$ = $V_{IH}$<br>$V_{IH/L}$ = $V_{IH}$ (min.) / $V_{IL}$ (max.)<br>Bank: inactive state | CKE = $V_{IH}$ | $I_{CC2S}$ | 10 | 10 | | |
| | CKE = $V_{IL}$<br>(Power Down mode) | $I_{CC2PS}$ | 2 | 2 | | |
| No Operating Current<br>$t_{CK}$ = min., $\overline{CS}$ = $V_{IH}$ (min.)<br>Bank: active state (2 Banks) | CKE = $V_{IH}$ | $I_{CC3}$ | 40 | 35 | | |
| | CKE = $V_{IL}$<br>(Power Down mode) | $I_{CC3P}$ | 10 | 10 | | |
| Burst Operating Current<br>($t_{CK}$ = min.)<br>Read/ Write command cycling | | $I_{CC4}$ | 110 | 100 | | 3, 4 |
| Auto Refresh Current<br>($t_{CK}$ = min.)<br>Auto refresh command cycling | | $I_{CC5}$ | 55 | 50 | | 3 |
| Self Refresh Current<br>(CKE = 0.2V)<br>Self refresh mode | | $I_{CC6}$ | 2 | 2 | mA | |

| PARAMETER | SYM. | MIN. | MAX. | UNIT | NOTES |
|---|---|---|---|---|---|
| Input Leakage Current<br>(0V ≤ $V_{IN}$ ≤ VCC, all other pins not under test = 0V) | $I_{I(L)}$ | -5 | 5 | µA | |
| Output Leakage Current<br>(Output disable , 0V ≤ $V_{OUT}$ ≤ VCCQ ) | $I_{O(L)}$ | -5 | 5 | µA | |
| LVTTL Output "H" Level Voltage<br>($I_{OUT}$ = -2 mA) | $V_{OH}$ | 2.4 | - | V | |
| LVTTL Output "L" Level Voltage<br>($I_{OUT}$ = 2 mA) | $V_{OL}$ | - | 0.4 | V | |

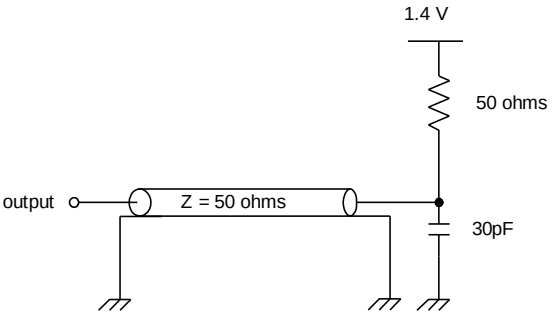
## 9.5 AC Characteristics

($V_{CC}$ = 3.3V ±0.3V for -6/-6I, $V_{CC}$ = 2.7V to 3.6V for -7, $T_A$ = 0 to 70°C for -6/-7, $T_A$= -40 to 85°C for -6I)

| PARAMETER | | SYM. | -6/-6I | | -7 | | UNIT | NOTES |
|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | | |
| Ref/Active to Ref/Active Command Period | | $t_{RC}$ | 60 | | 65 | | nS | |
| Active to Precharge Command Period | | $t_{RAS}$ | 42 | 100000 | 45 | 100000 | | |
| Active to Read/Write Command Delay Time | | $t_{RCD}$ | 18 | | 20 | | | |
| Read/Write(a) to Read/Write(b)Command Period | | $t_{CCD}$ | 1 | | 1 | | $t_{CK}$ | |
| Precharge to Active(b) Command Period | | $t_{RP}$ | 18 | | 18 | | nS | |
| Active(a) to Active(b) Command Period | | $t_{RRD}$ | 12 | | 14 | | | |
| Write Recovery Time | CL* = 2 | $t_{WR}$ | 2 | | 2 | | $t_{CK}$ | |
| | CL* = 3 | | 2 | | 2 | | | |
| CLK Cycle Time | CL* = 2 | $t_{CK}$ | 8 | 1000 | 10 | 1000 | nS | |
| | CL* = 3 | | 6 | 1000 | 7 | 1000 | | |
| CLK High Level Width | | $t_{CH}$ | 2 | | 2 | | | 8 |
| CLK Low Level Width | | $t_{CL}$ | 2 | | 2 | | | 8 |
| Access Time from CLK | CL* = 2 | $t_{AC}$ | | 5.5 | | 5.5 | | 9 |
| | CL* = 3 | | | 5 | | 5 | | 9 |
| Output Data Hold Time | | $t_{OH}$ | 2 | | 2 | | | 9 |
| Output Data High Impedance Time | | $t_{HZ}$ | 2 | 6 | 2.5 | 7 | | 7 |
| Output Data Low Impedance Time | | $t_{LZ}$ | 0 | | 0 | | | 9 |
| Power Down Mode Entry Time | | $t_{SB}$ | 0 | 6 | 0 | 7 | | |
| Data-in-Set-up Time | | $t_{DS}$ | 1.5 | | 1.5 | | | 8 |
| Data-in Hold Time | | $t_{DH}$ | 0.7 | | 1 | | | 8 |
| Address Set-up Time | | $t_{AS}$ | 1.5 | | 1.5 | | | 8 |
| Address Hold Time | | $t_{AH}$ | 0.7 | | 1 | | | 8 |
| CKE Set-up Time | | $t_{CKS}$ | 1.5 | | 1.5 | | | 8 |
| CKE Hold Time | | $t_{CKH}$ | 0.7 | | 1 | | | 8 |
| Command Set-up Time | | $t_{CMS}$ | 1.5 | | 1.5 | | | 8 |
| Command Hold Time | | $t_{CMH}$ | 0.7 | | 1 | | | 8 |
| Refresh Time | | $t_{REF}$ | | 64 | | 64 | mS | |
| Mode Register Set Cycle Time | | $t_{RSC}$ | 2 | | 2 | | $t_{CK}$ | |
| Exit self refresh to ACTIVE command | | $t_{XSR}$ | 72 | | 75 | | nS | |

**Notes:**

1. Operation exceeds "Absolute Maximum Ratings" may cause permanent damage to the devices.
2. All voltages are referenced to $V_{SS}$.
   - 2.7V~3.6V power supply for -7 speed grade.
   - 3.3V ± 0.3V power supply for -6/-6I speed grades.
3. These parameters depend on the cycle rate and listed values are measured at a cycle rate with the minimum values of $t_{CK}$ and $t_{RC}$.
4. These parameters depend on the output loading conditions. Specified values are obtained with output open.
5. Power up sequence please refer to "Functional Description" section described before.
6. AC Test Load diagram.

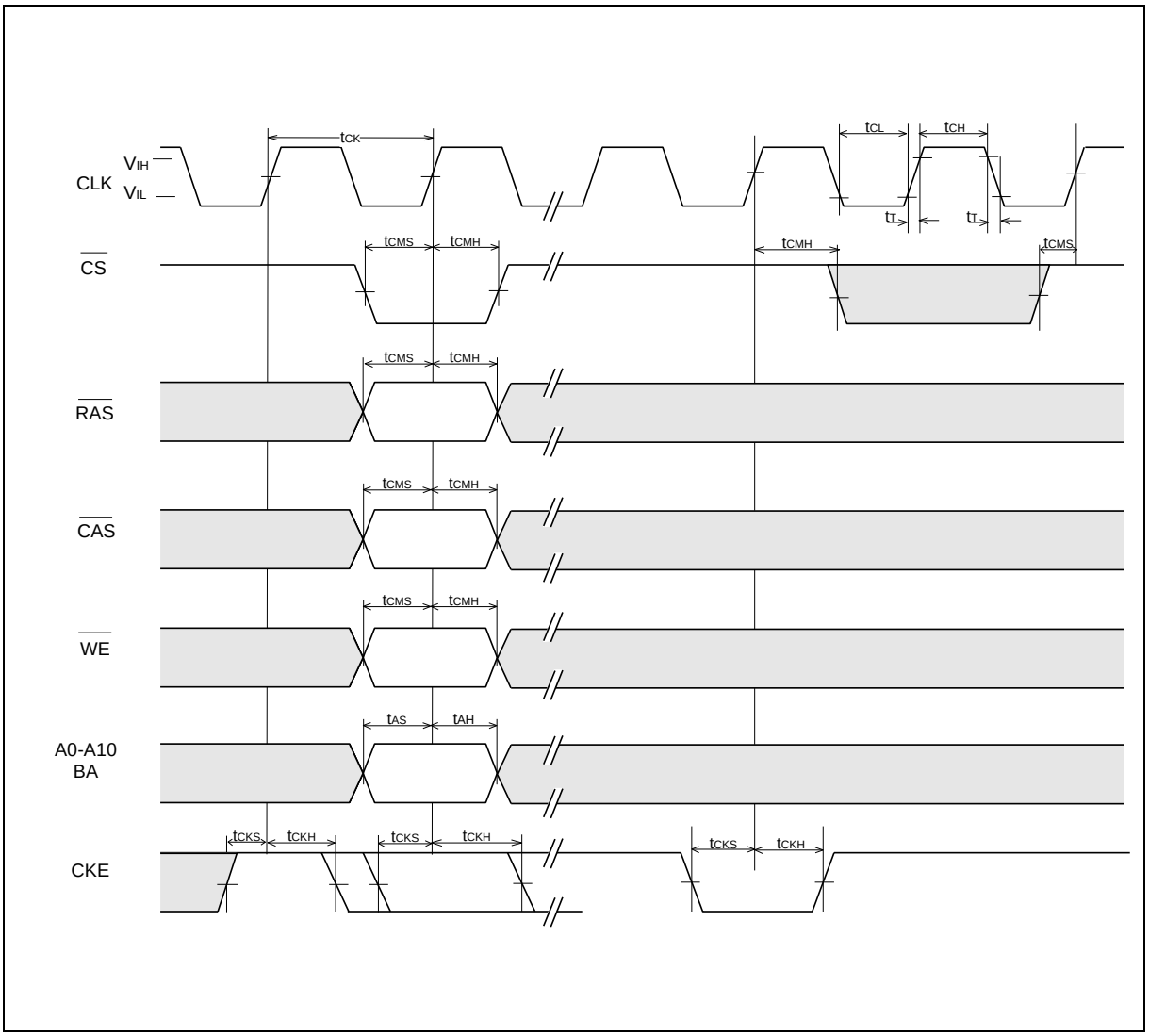



AC TEST LOAD

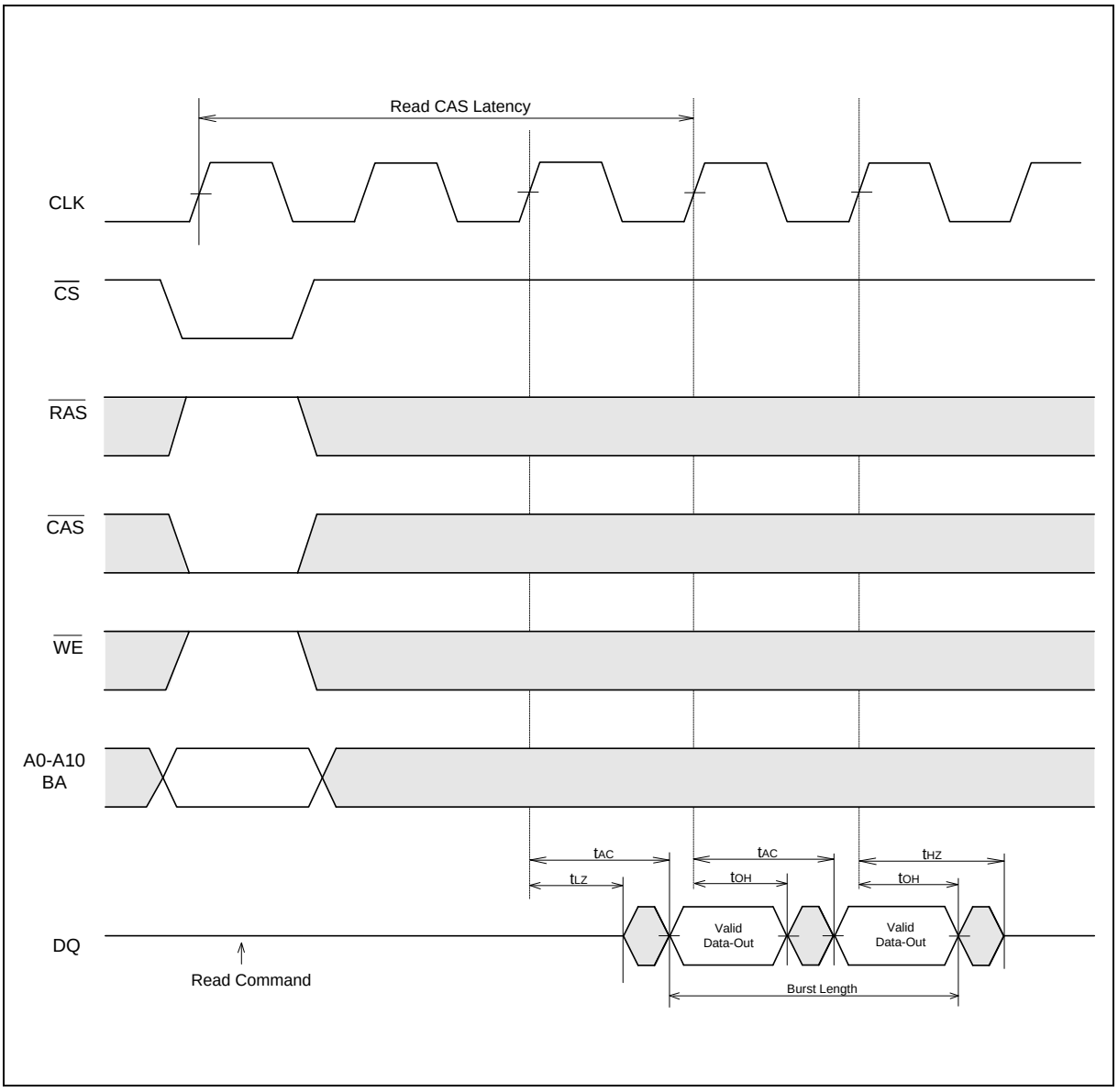
7. $t_{HZ}$ defines the time at which the outputs achieve the open circuit condition and is not referenced to output level.
8. Assumed input rise and fall time ($t_T$ ) = 1nS.
   If tr & tf is longer than 1nS, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]nS should be added to the parameter
   ( The $t_T$ maximum can't be more than 10nS for low frequency application. )
9. If clock rising time ($t_T$) is longer than 1nS, ($t_T$ /2-0.5)nS should be added to the parameter.

# 10. TIMING WAVEFORMS

## 10.1 Command Input Timing



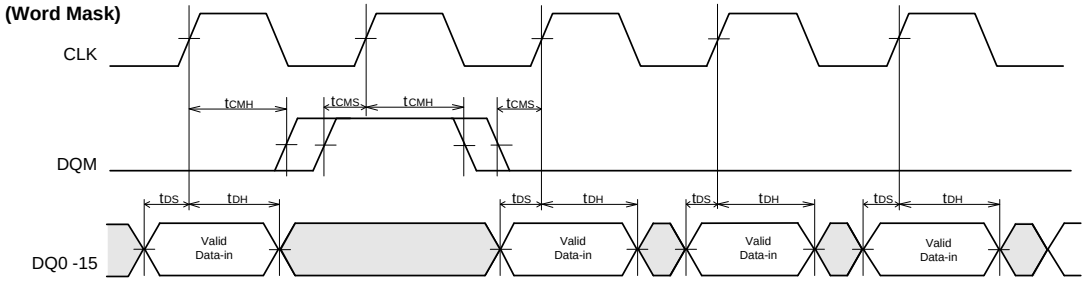
## 10.2 Read Timing



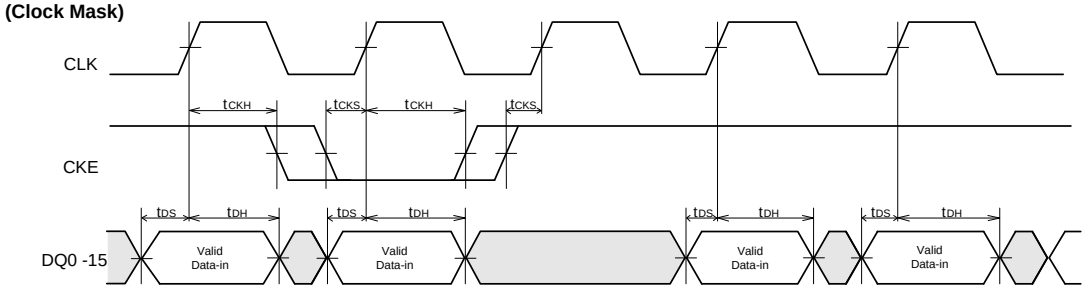
## 10.3 Control Timing of Input/Output Data

### Control Timing of Input Data

**(Word Mask)**

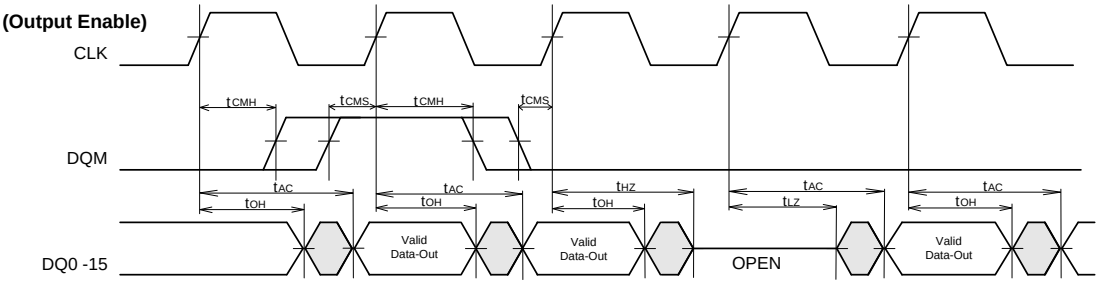



**(Clock Mask)**

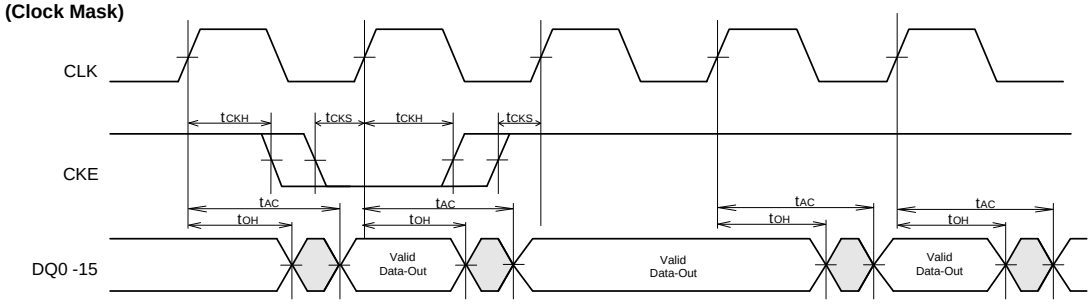



### Control Timing of Output Data

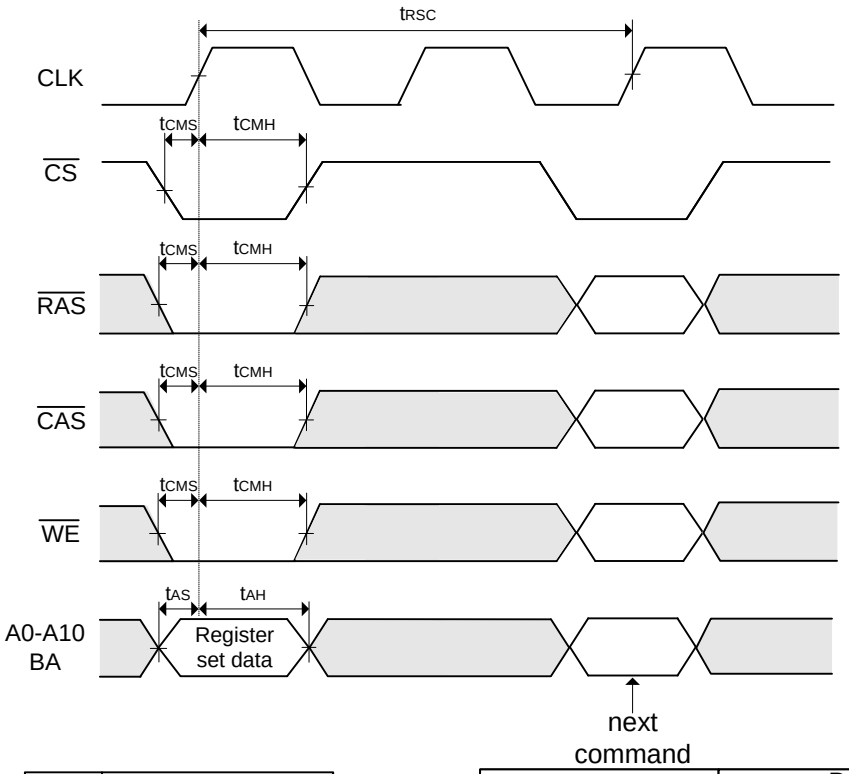
**(Output Enable)**




**(Clock Mask)**



## 10.4 Mode Register Set Cycle




| | | |
|---|---|---|
| A0 | Burst Length | |
| A1 | | |
| A2 | | |
| A3 | Addressing Mode | |
| A4 | CAS Latency | |
| A5 | | |
| A6 | | |
| A7 | "0" | (Test Mode) |
| A8 | "0" | Reserved |
| A9 | Write Mode | |
| A10 | "0" | Reserved |
| BA | "0" | |

| | | | Burst Length | |
|---|---|---|---|---|
| A2 | A1 | A0 | Sequential | Interleave |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | Reserved | Reserved |
| 1 | 0 | 1 | | |
| 1 | 1 | 0 | | |
| 1 | 1 | 1 | Full Page | |

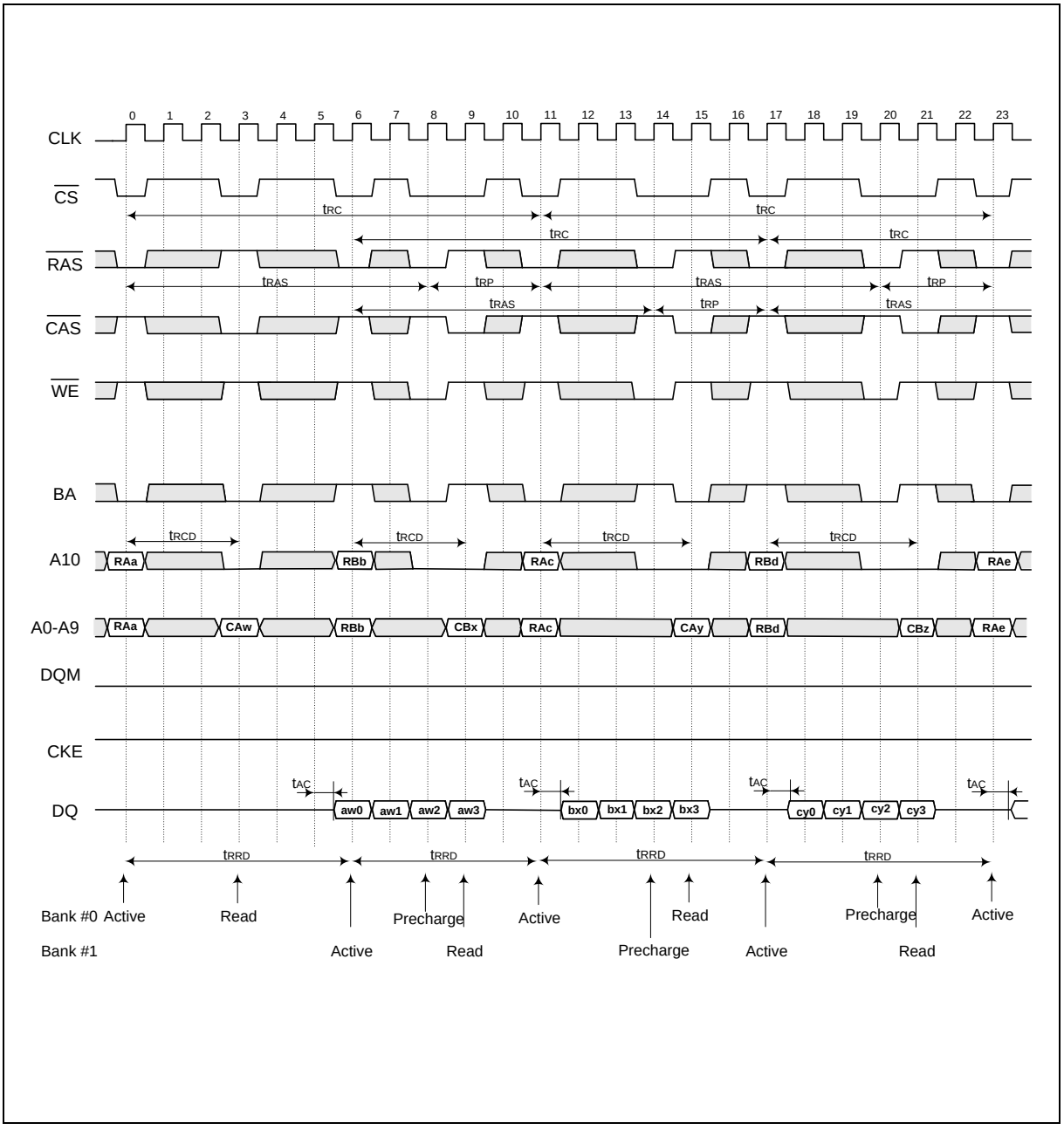
| A3 | Addressing Mode |
|---|---|
| 0 | Sequential |
| 1 | Interleave |

| A6 | A5 | A4 | CAS Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | Reserved |

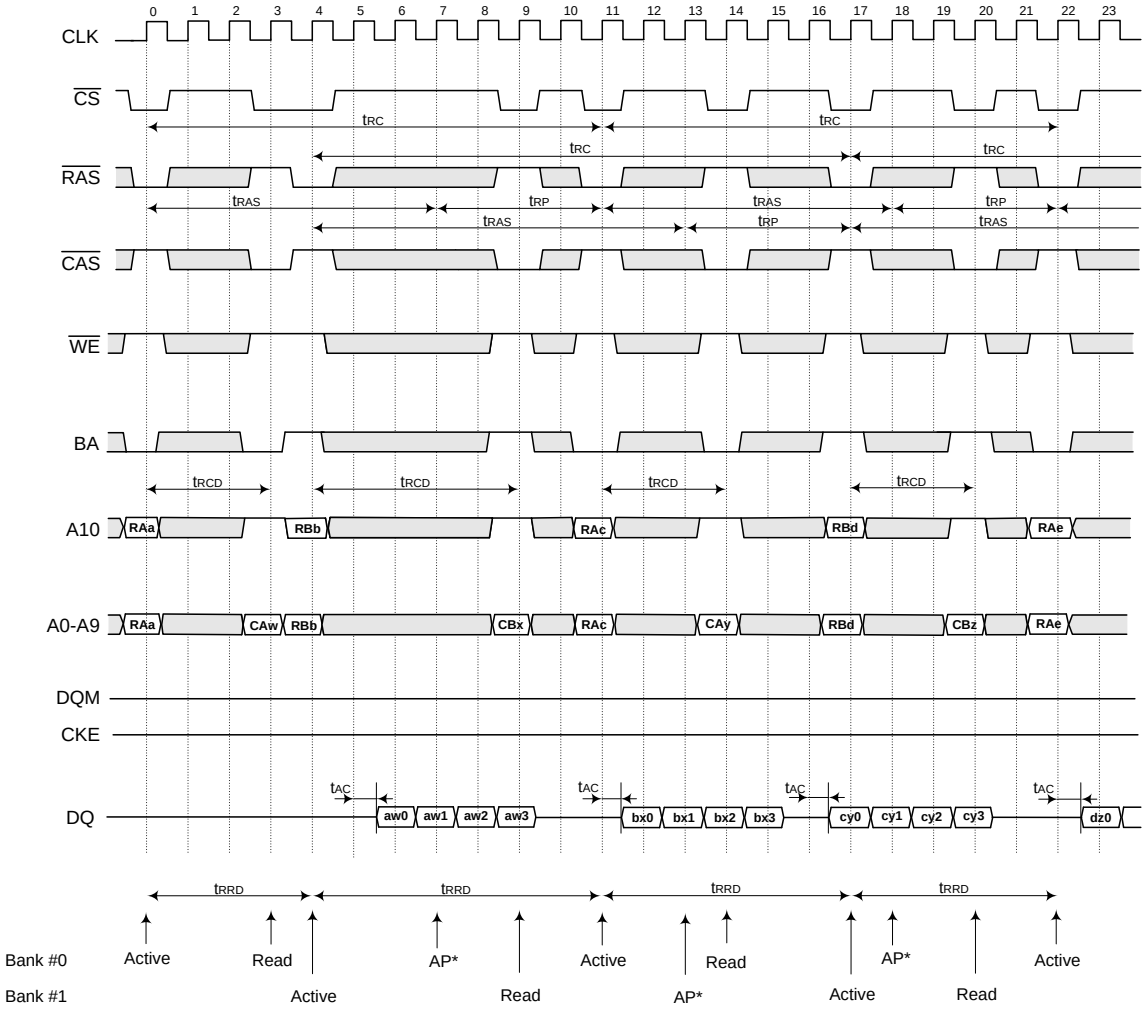
| A9 | Single Write Mode |
|---|---|
| 0 | Burst read and Burst write |
| 1 | Burst read and single write |

## 11. OPERATING TIMING EXAMPLE

### 11.1 Interleaved Bank Read (Burst Length = 4, CAS Latency = 3)

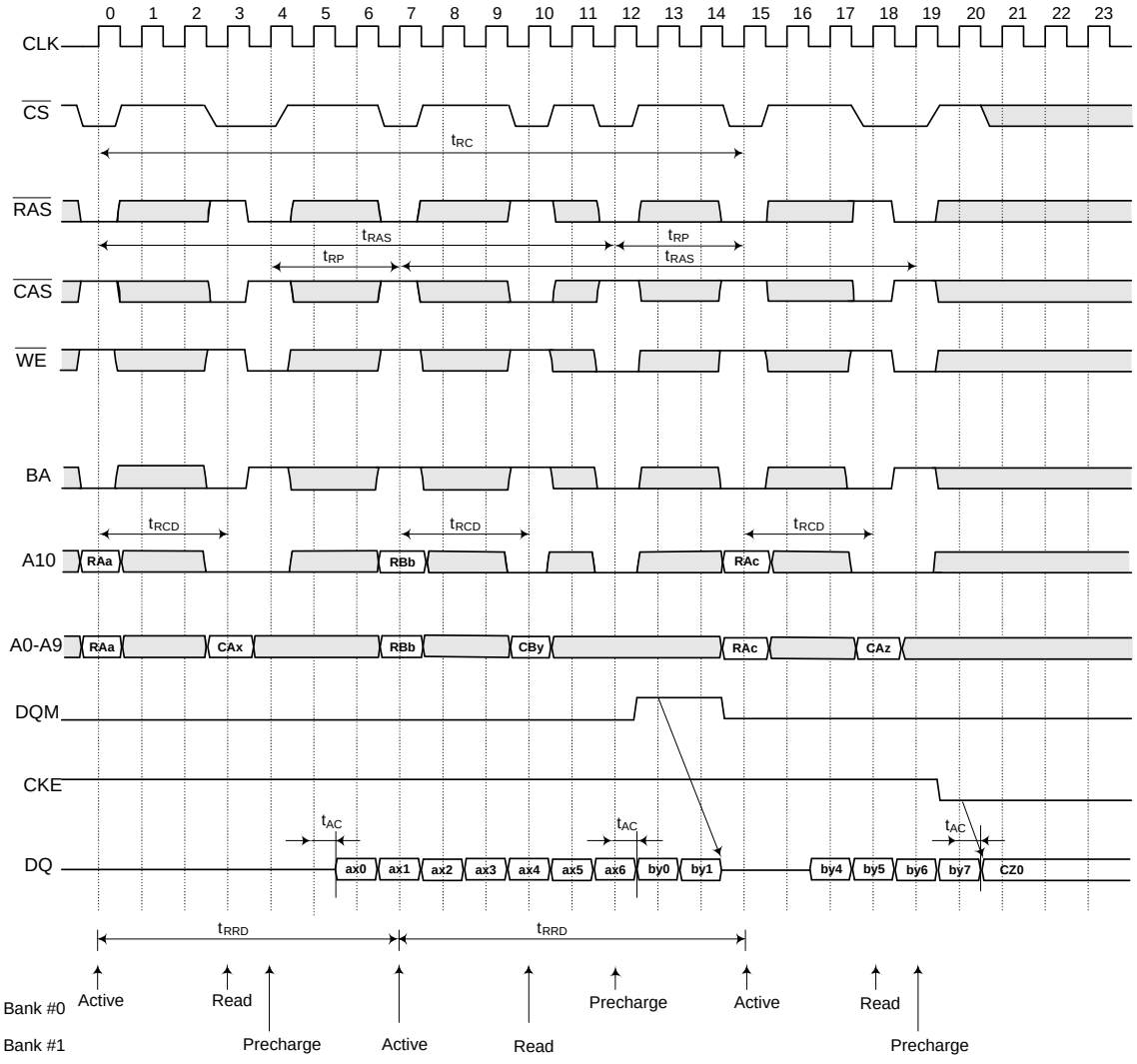


## 11.2 Interleaved Bank Read (Burst Length = 4, CAS Latency = 3, Auto-precharge)

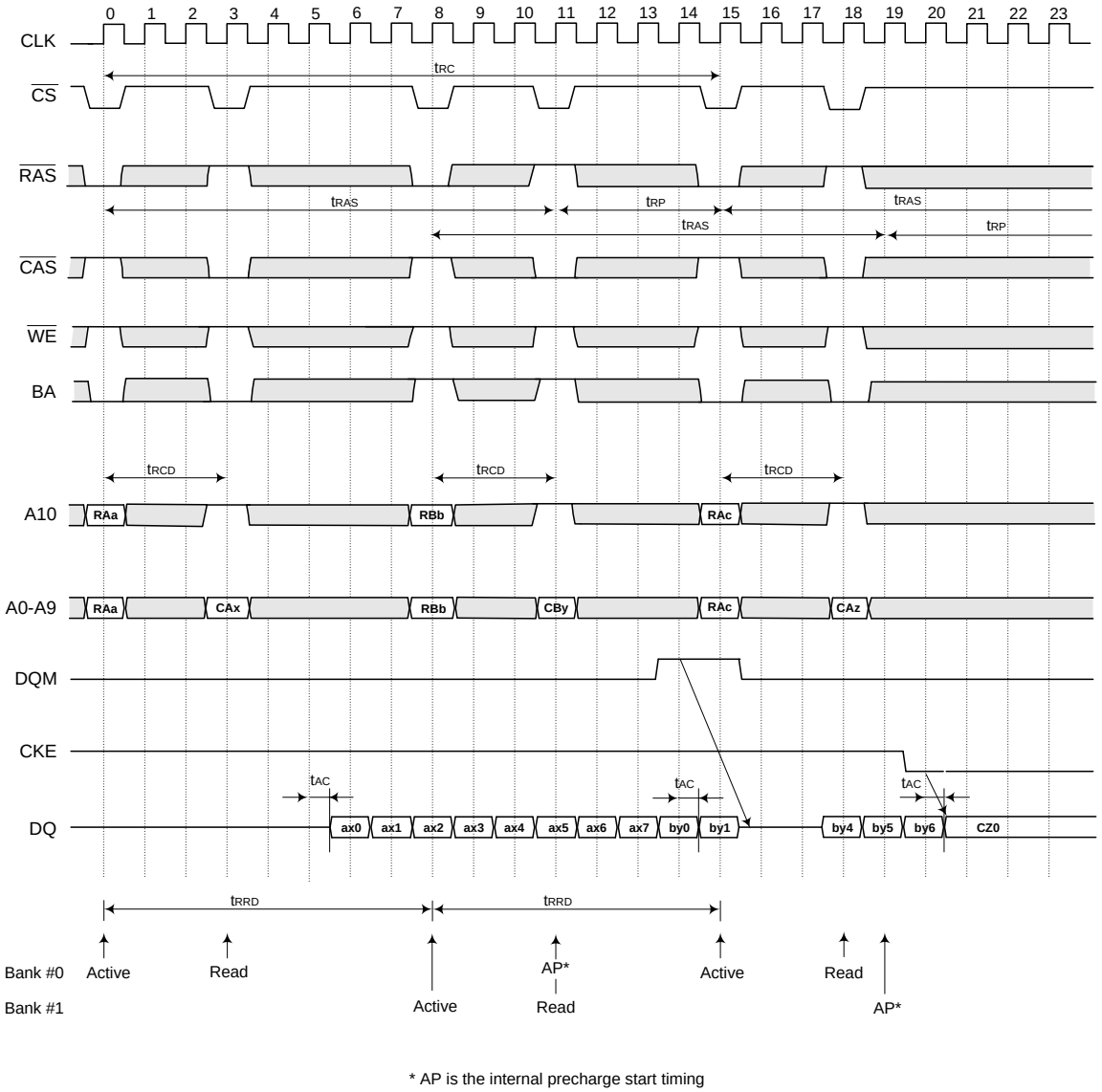



* AP is the internal precharge start timing

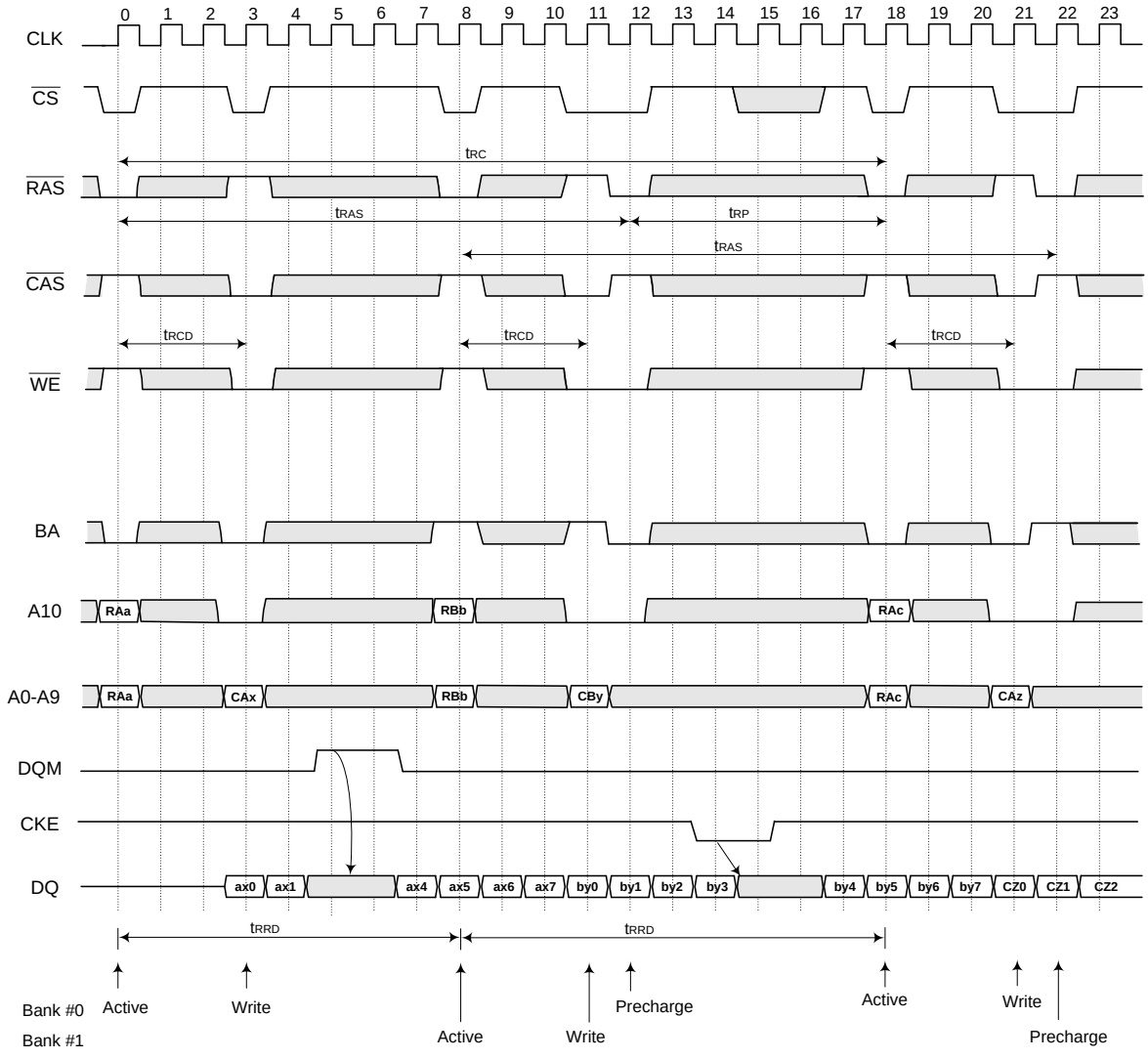
## 11.3 Interleaved Bank Read (Burst Length = 8, CAS Latency = 3)



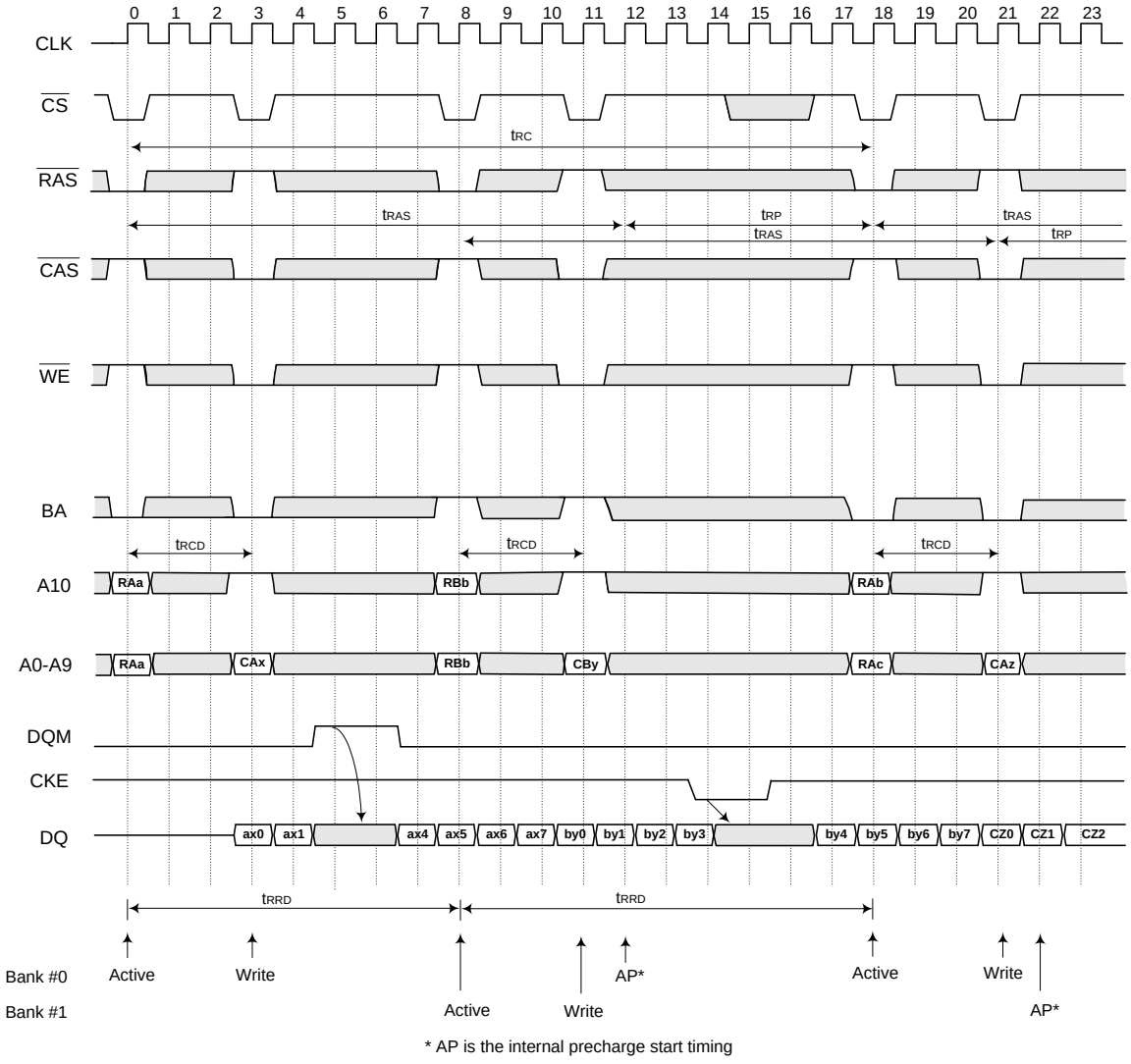
## 11.4 Interleaved Bank Read (Burst Length = 8, CAS Latency = 3, Auto-precharge)



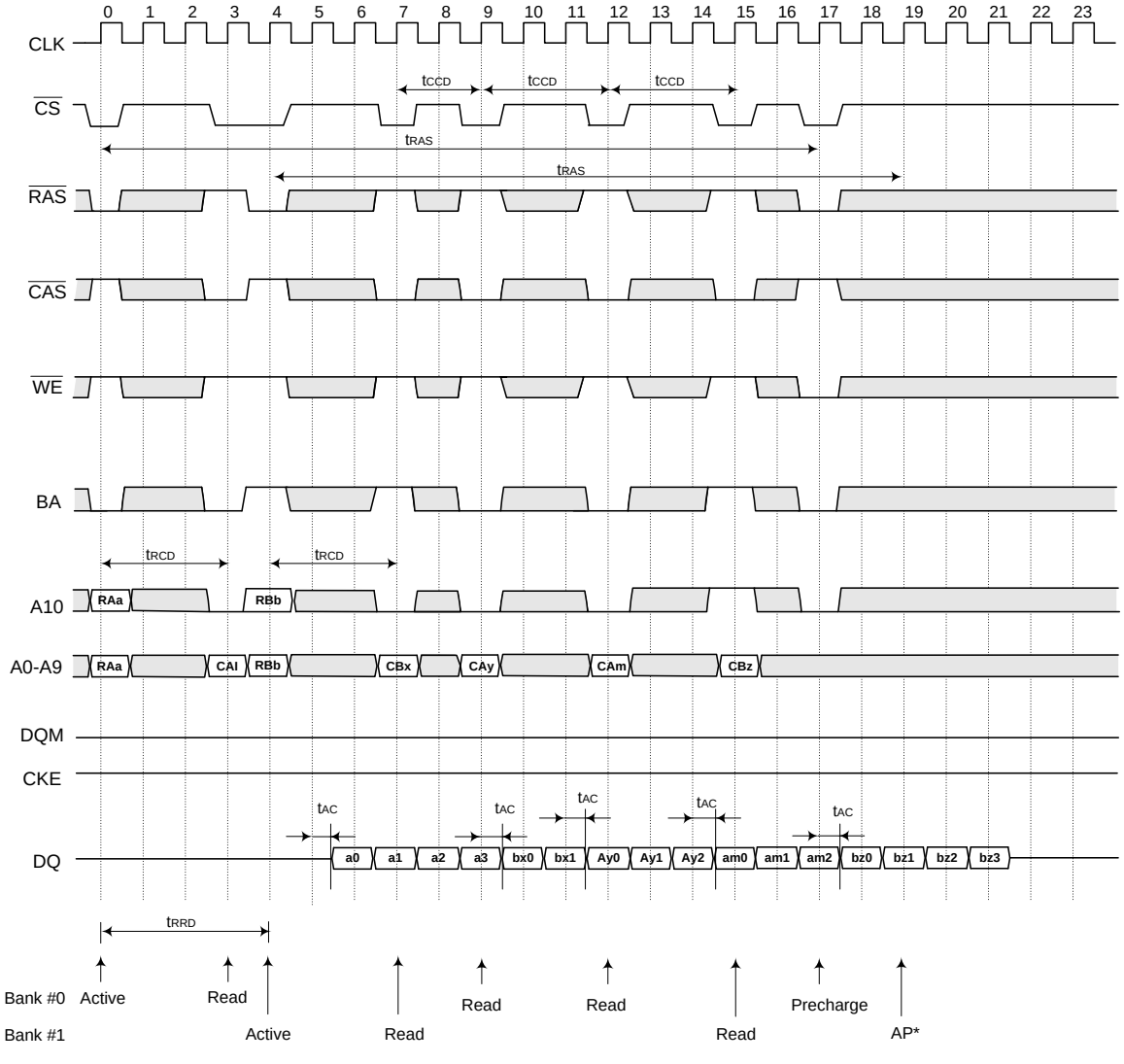
## 11.5 Interleaved Bank Write (Burst Length = 8)



## 11.6 Interleaved Bank Write (Burst Length = 8, Auto-precharge)

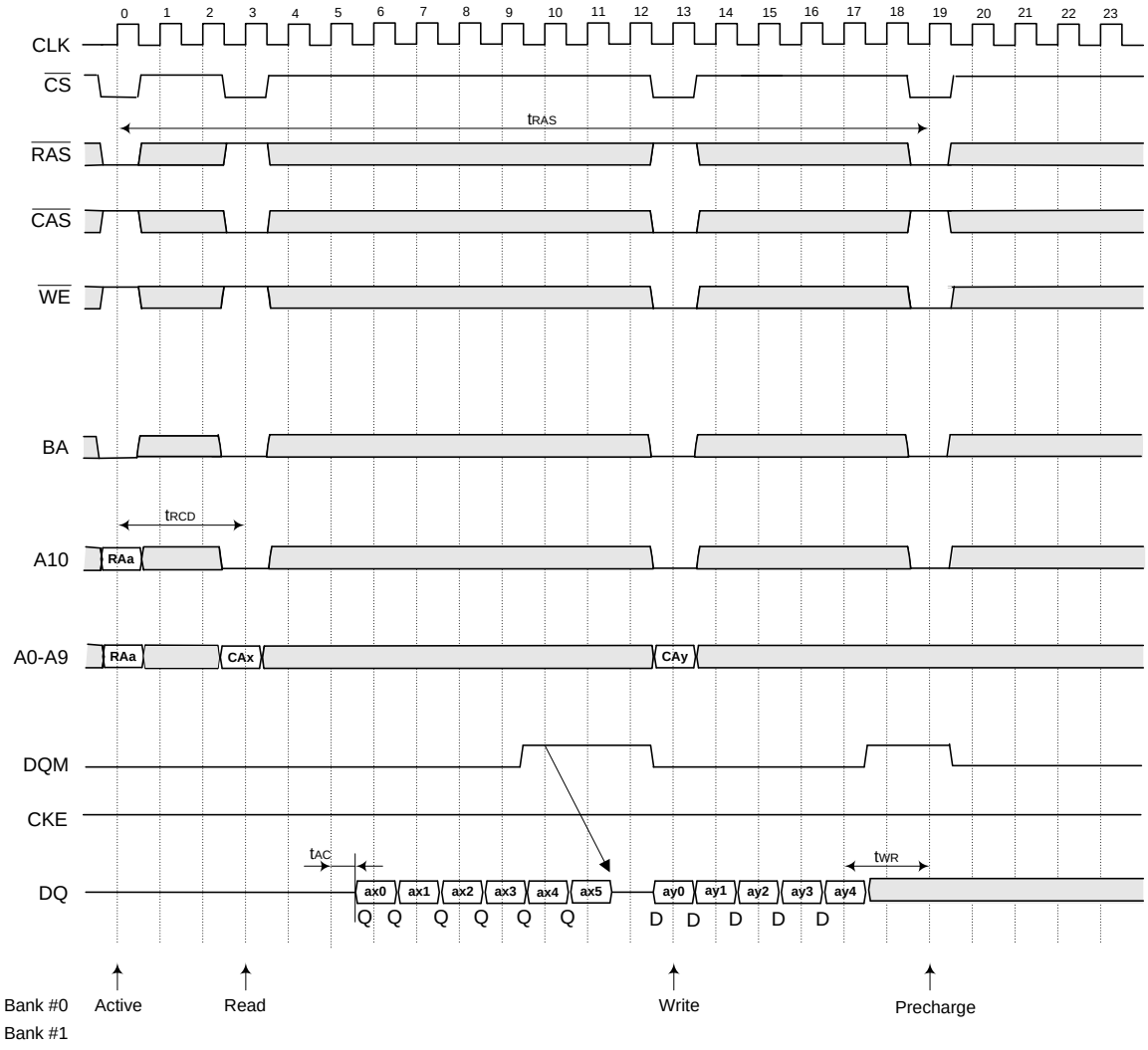


## 11.7 Page Mode Read (Burst Length = 4, CAS Latency = 3)

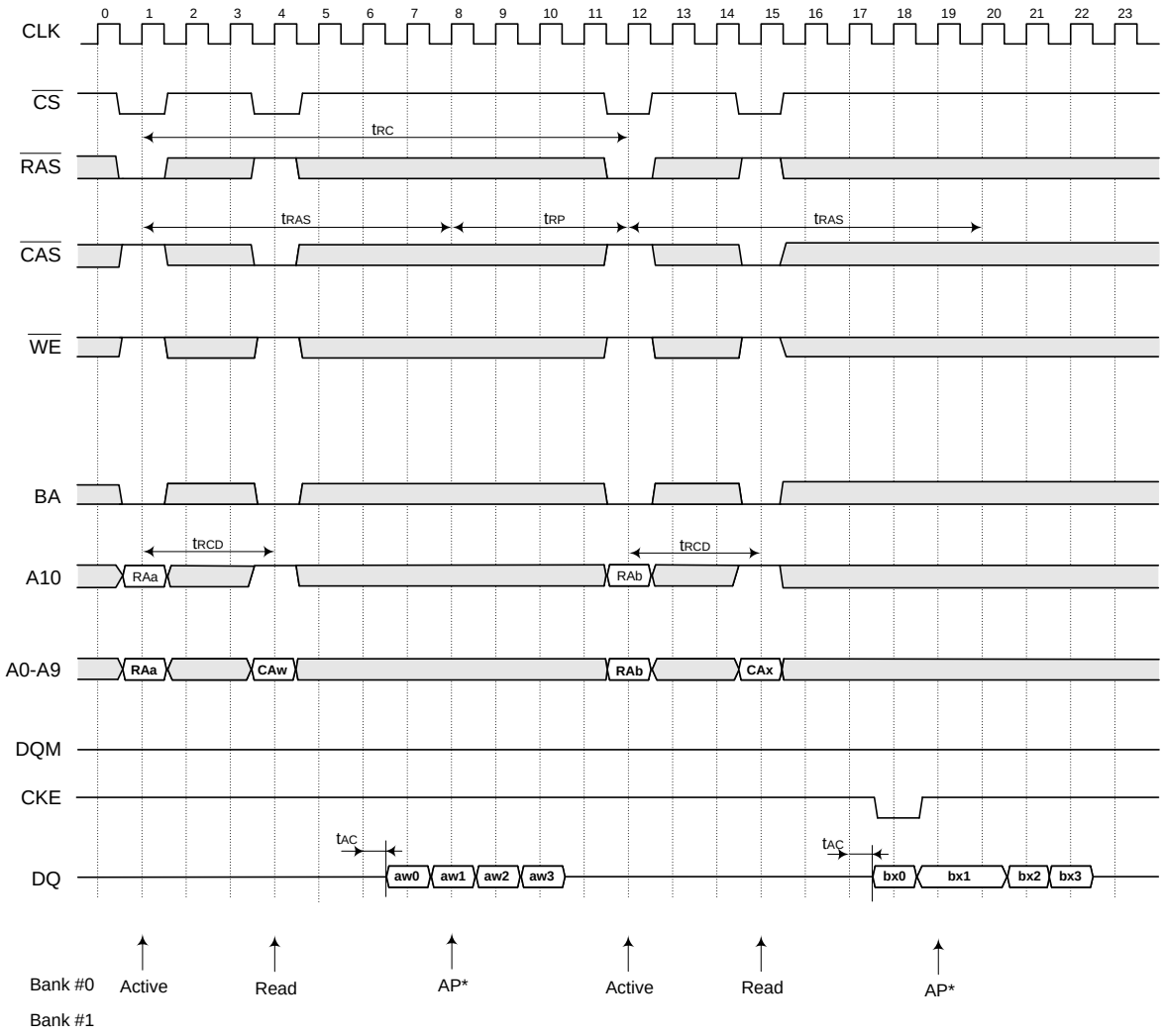



* AP is the internal precharge start timing

## 11.8 Page Mode Read / Write (Burst Length = 8, CAS Latency = 3)

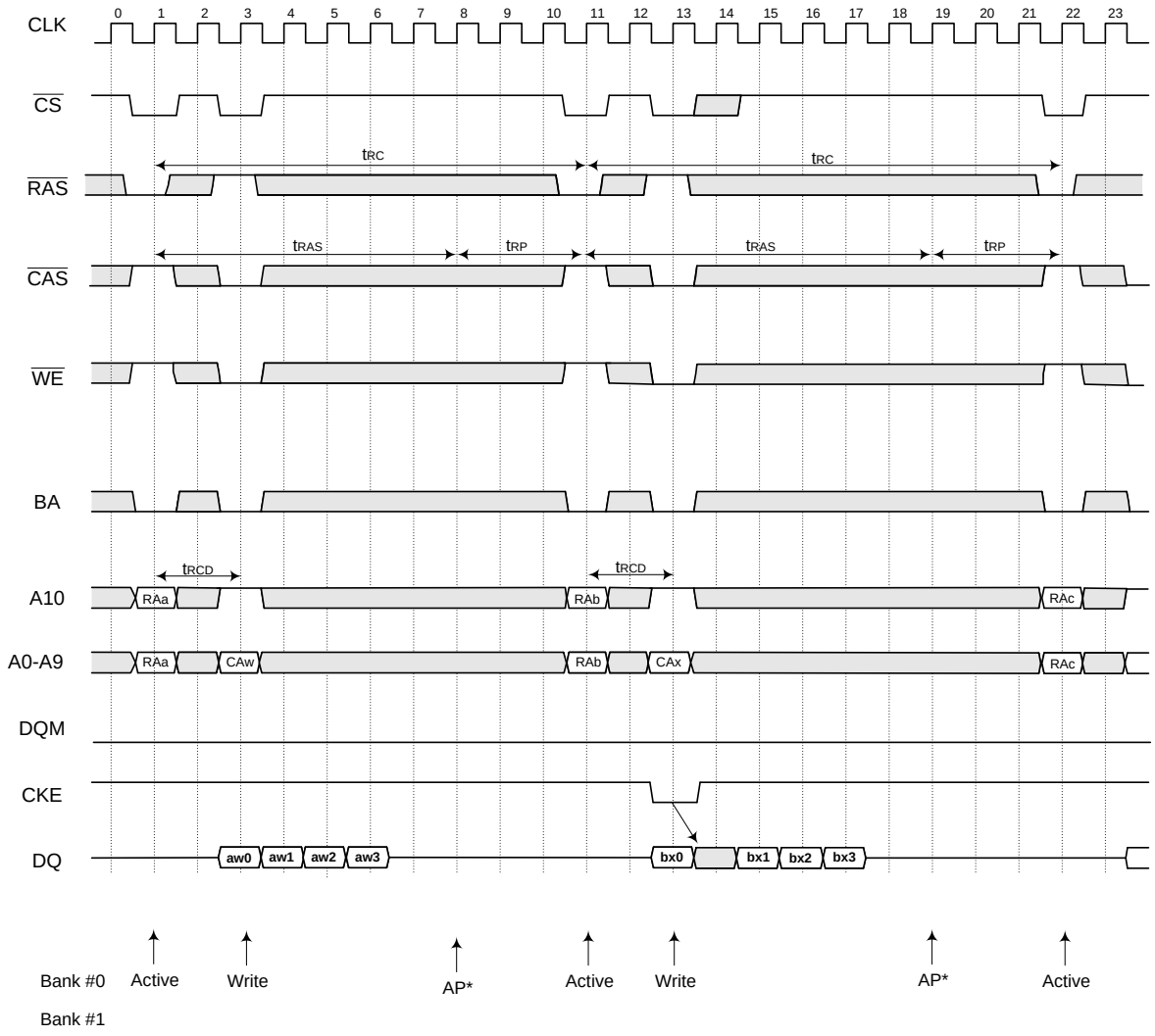


## 11.9 Auto Precharge Read (Burst Length = 4, CAS Latency = 3)



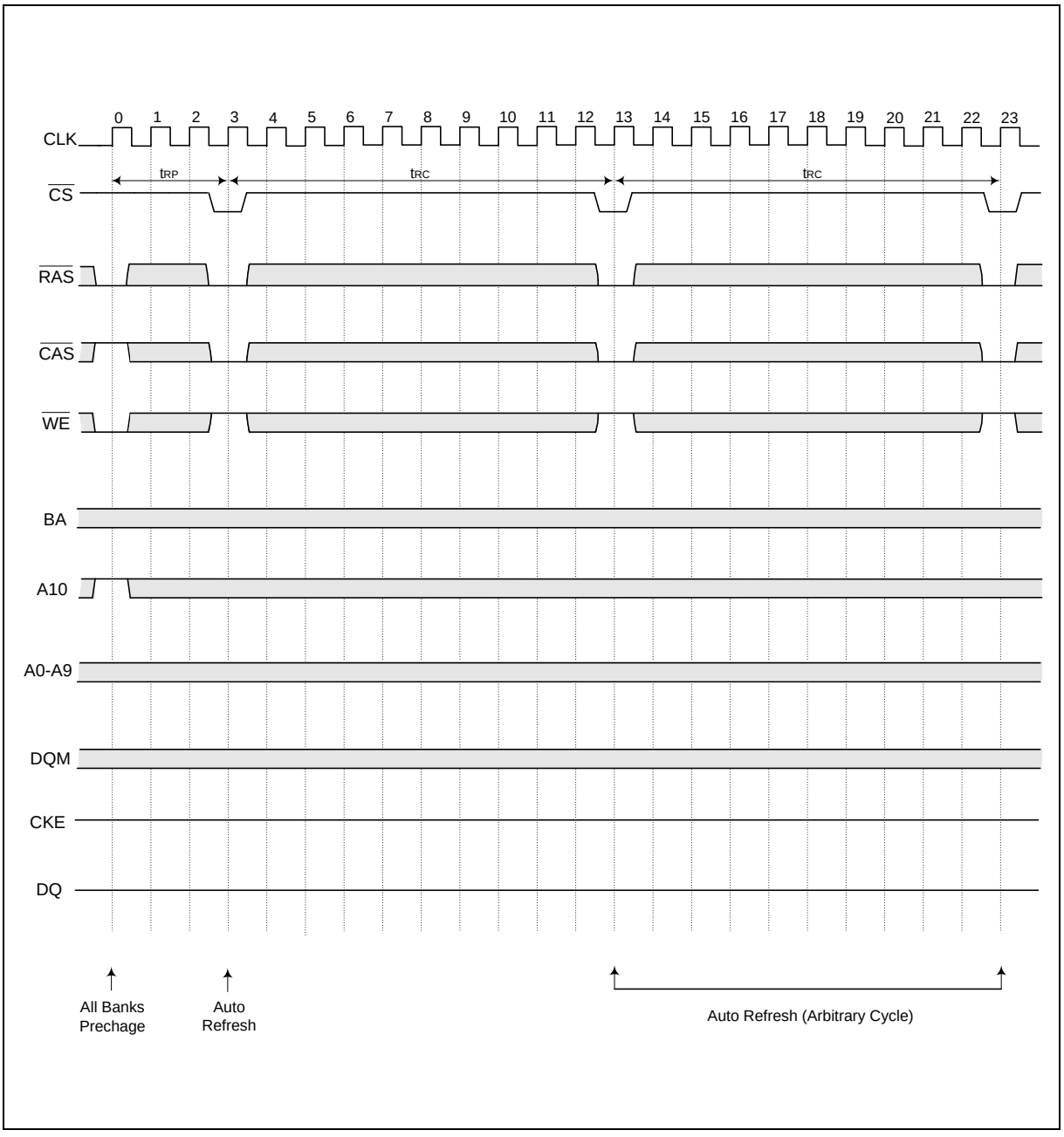

* AP is the internal precharge start timing

## 11.10 Auto Precharge Write (Burst Length = 4)

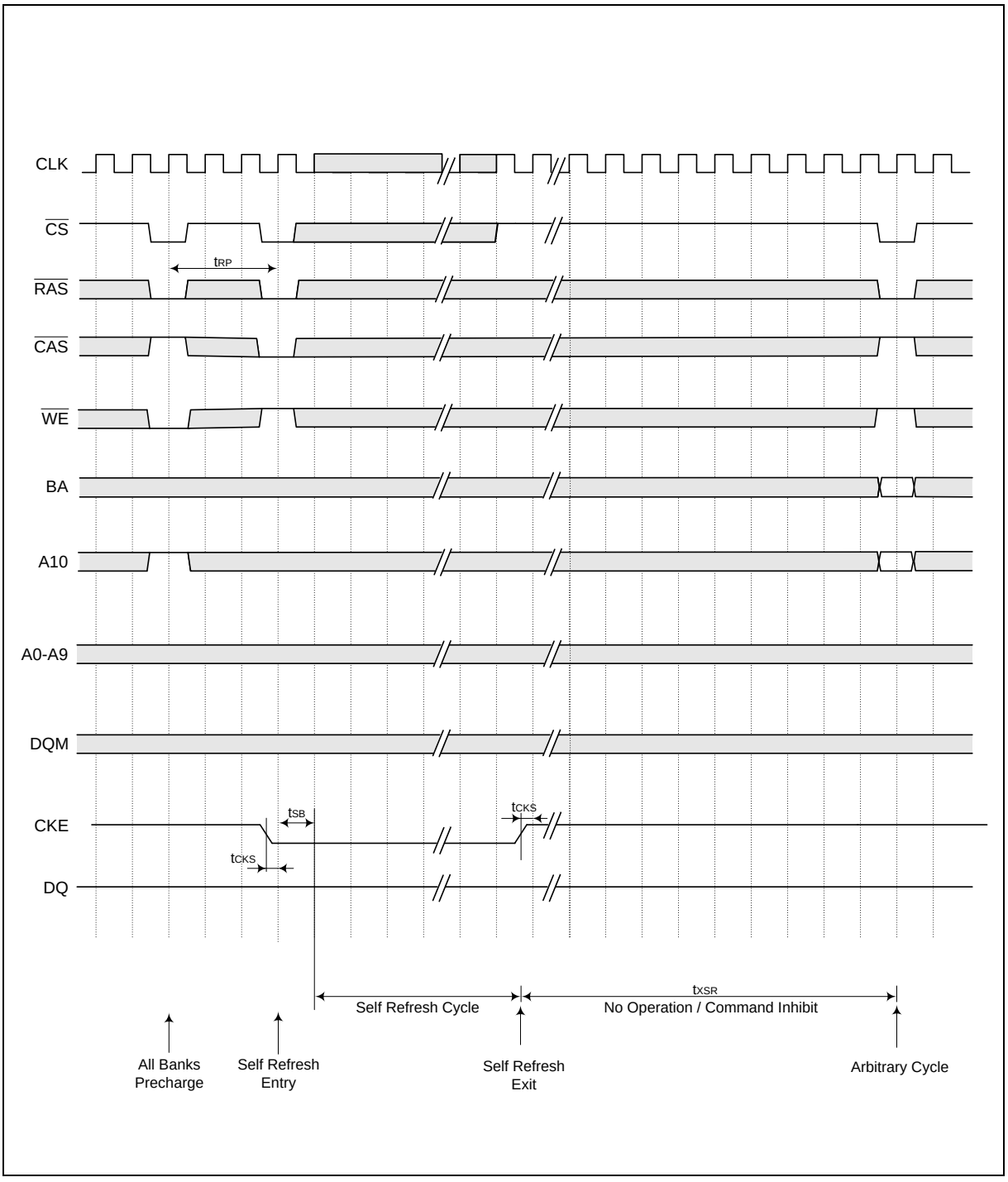



* AP is the internal precharge start timing

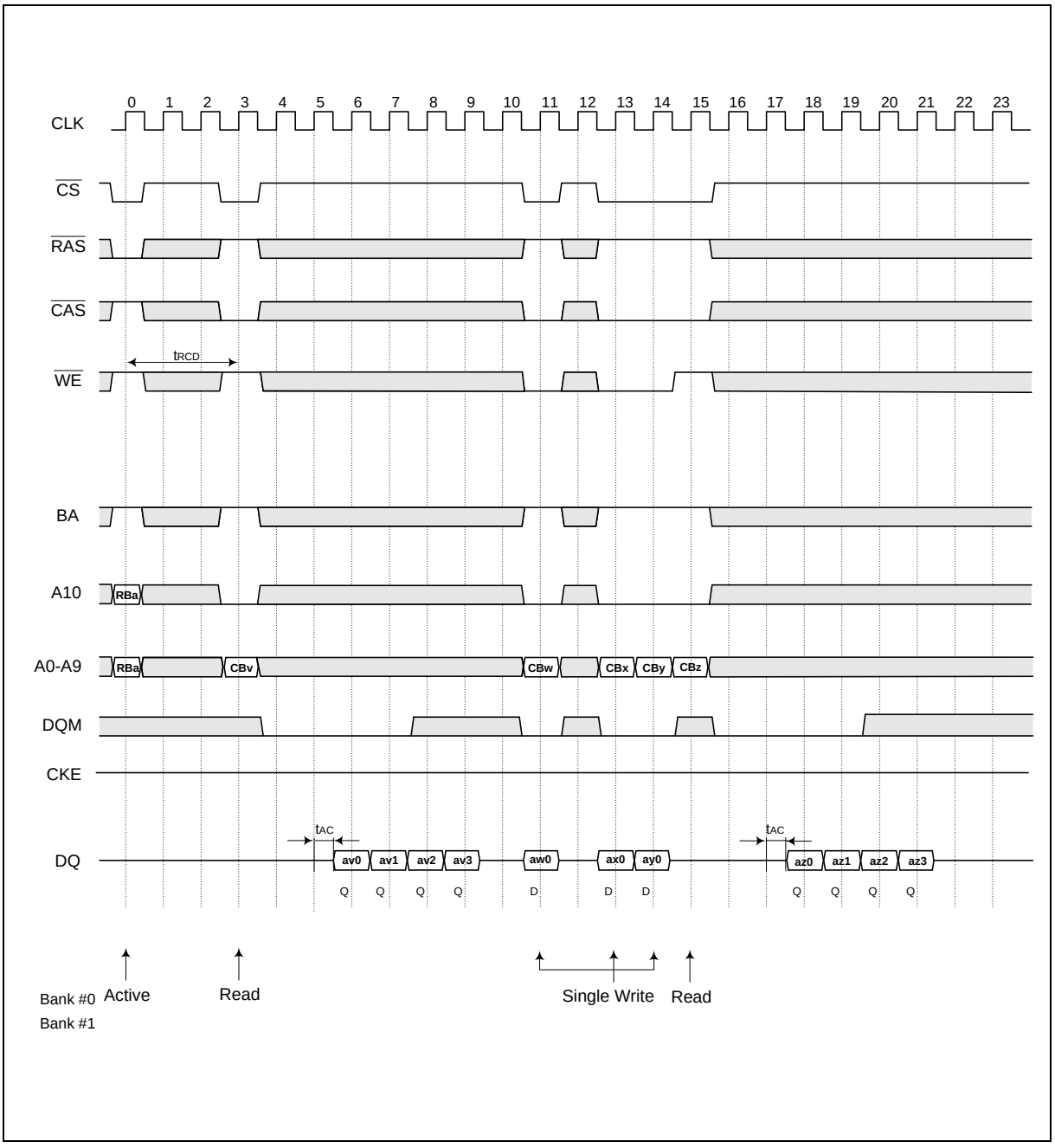
## 11.11 Auto Refresh Cycle



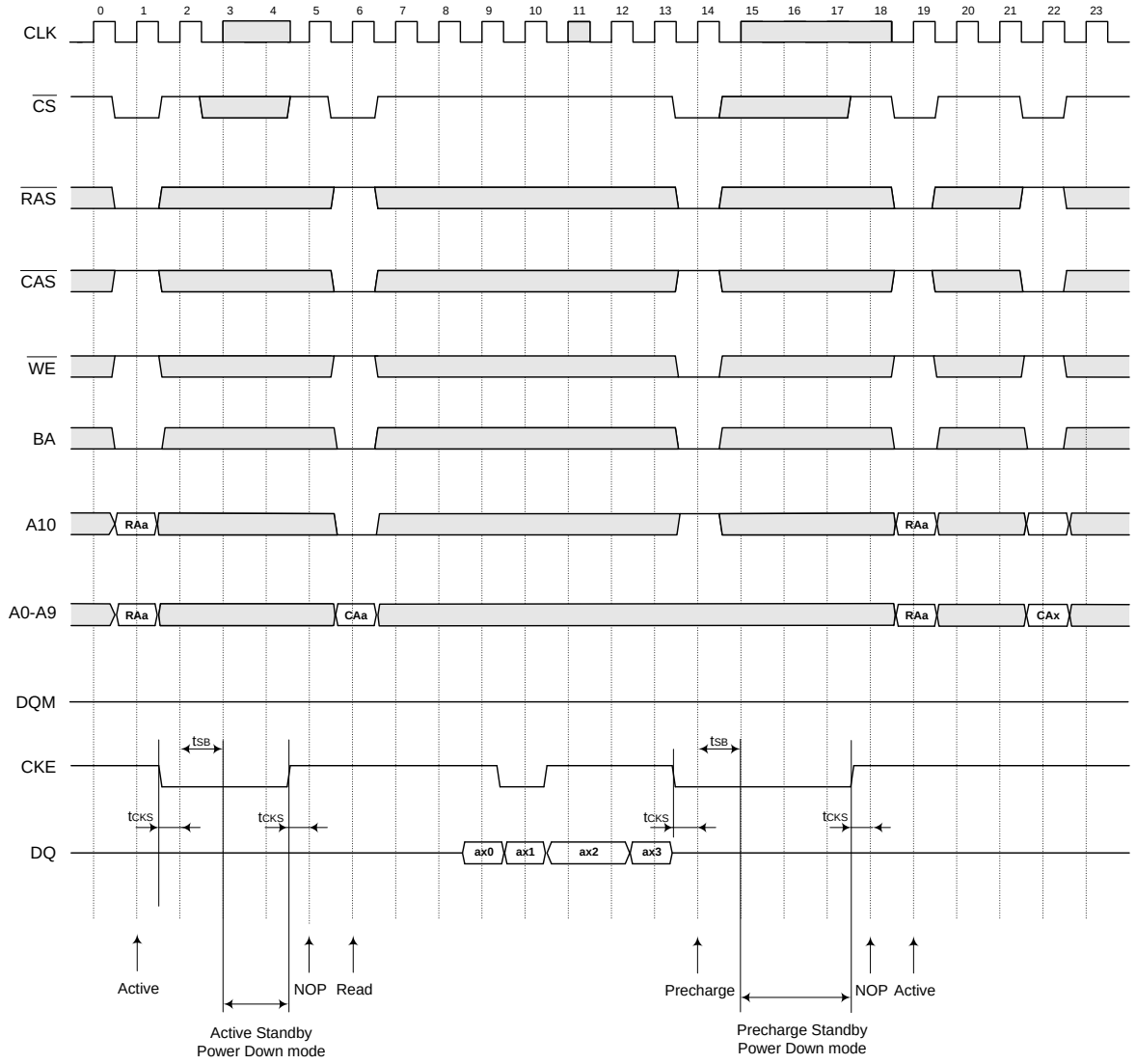
## 11.12 Self Refresh Cycle



## 11.13 Burst Read and Single Write (Burst Length = 4, CAS Latency = 3)

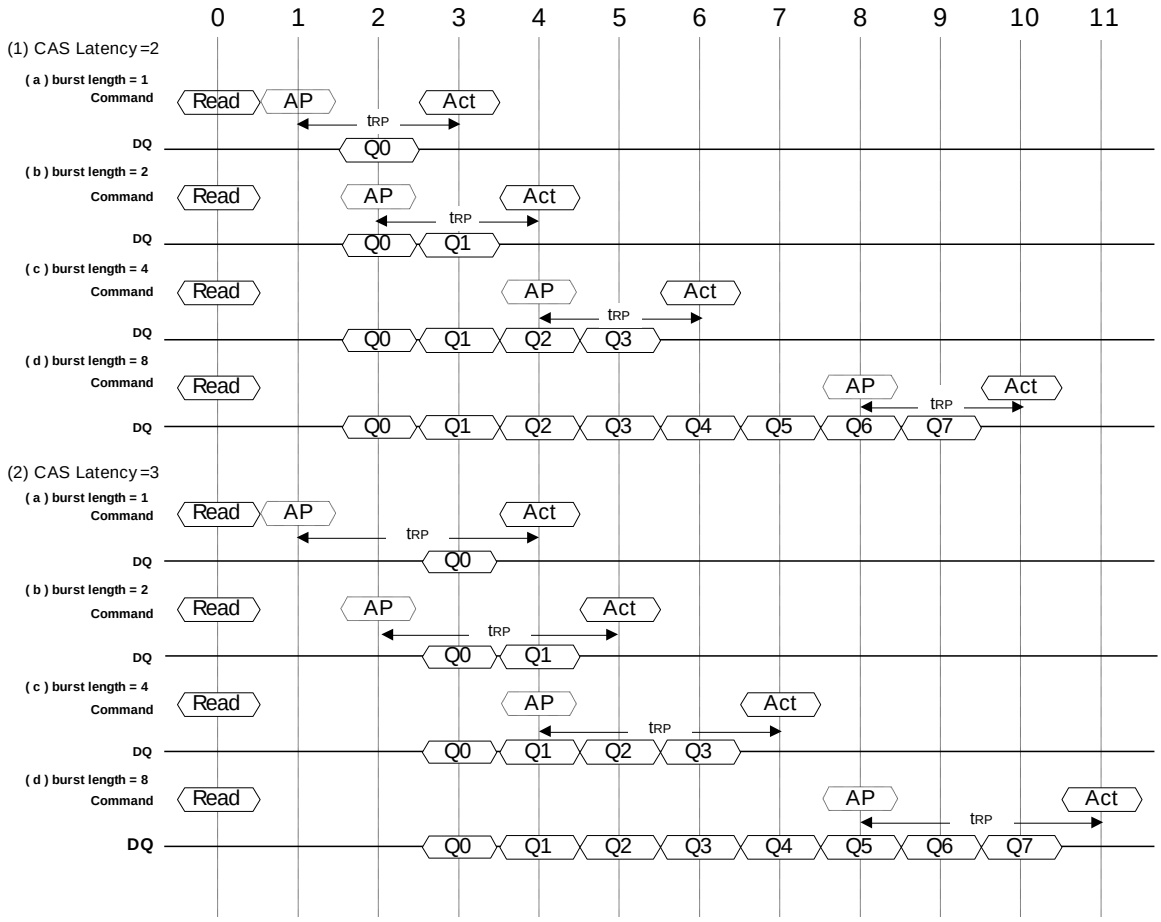


## 11.14 Power Down Mode




Note: The PowerDown Mode is entered by asserting CKE "low".
All Input/Output buffers (except CKE buffers) are turned off in the Power Down mode.
When CKE goes high, command input must be No operation at next CLK rising edge.
Violating refresh requirements during power-down may result in a loss of data.

## 11.15 Auto-precharge Timing (Read Cycle)

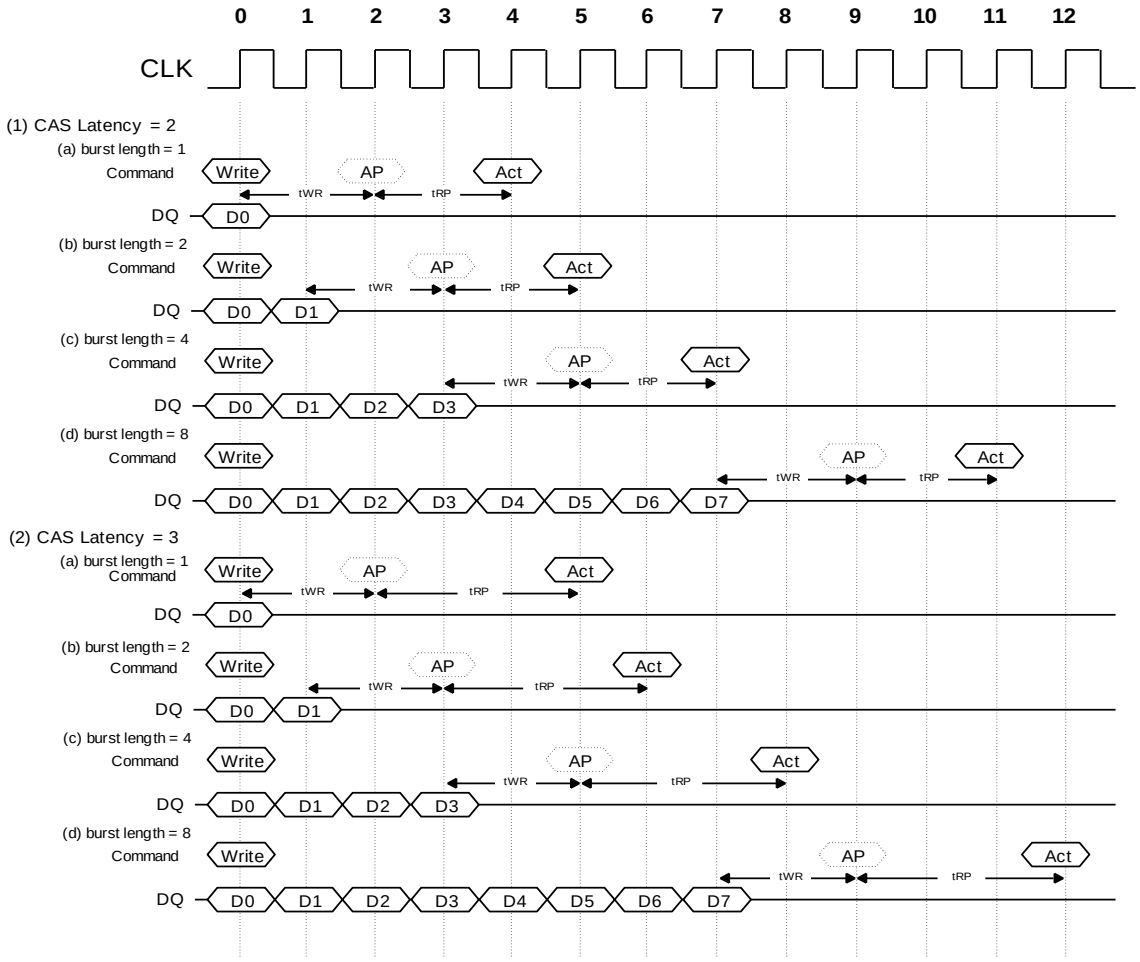



Note:

| | |
|---|---|
| Read | represents the Read with Auto precharge command. |
| AP | represents the start of internal precharging. |
| Act | represents the Bank Activate command. |

When the Auto precharge command is asserted, the period from Bank Activate command to the start of internal precgarging must be at least $t_{RAS}$ (min).

## 11.16 Auto-precharge Timing (Write Cycle)

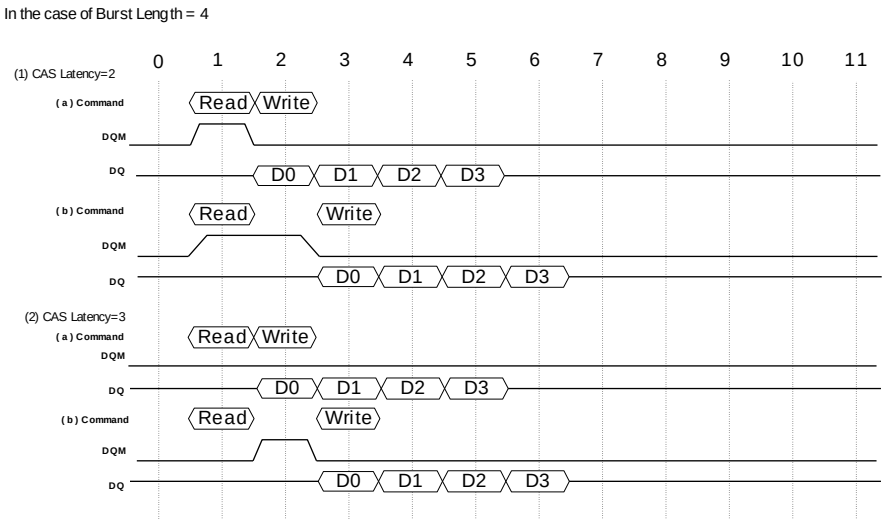



Note )

| | |
|---|---|
| Write | represents the Write with Auto precharge command. |
| AP | represents the start of internal precharing. |
| Act | represents the Bank Active command. |

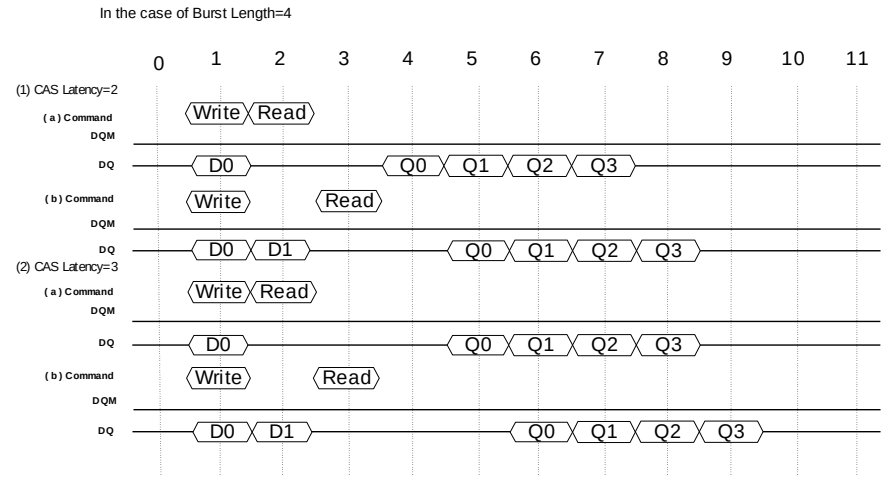
When the /auto precharge command is asserted,the period from Bank Activate command to the start of intermal precgarging must be at least tRAS (min).

## 11.17 Timing Chart of Read to Write Cycle

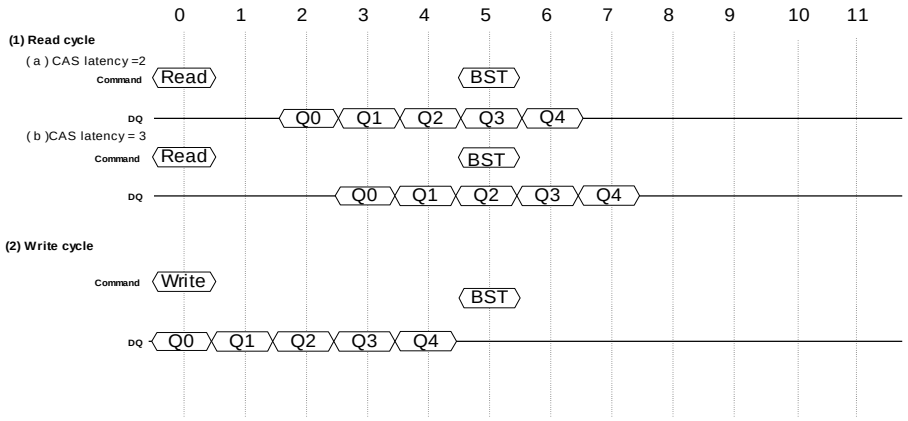



Note: The Output data must be masked by DQM to avoid I/O conflict

## 11.18 Timing Chart of Write to Read Cycle

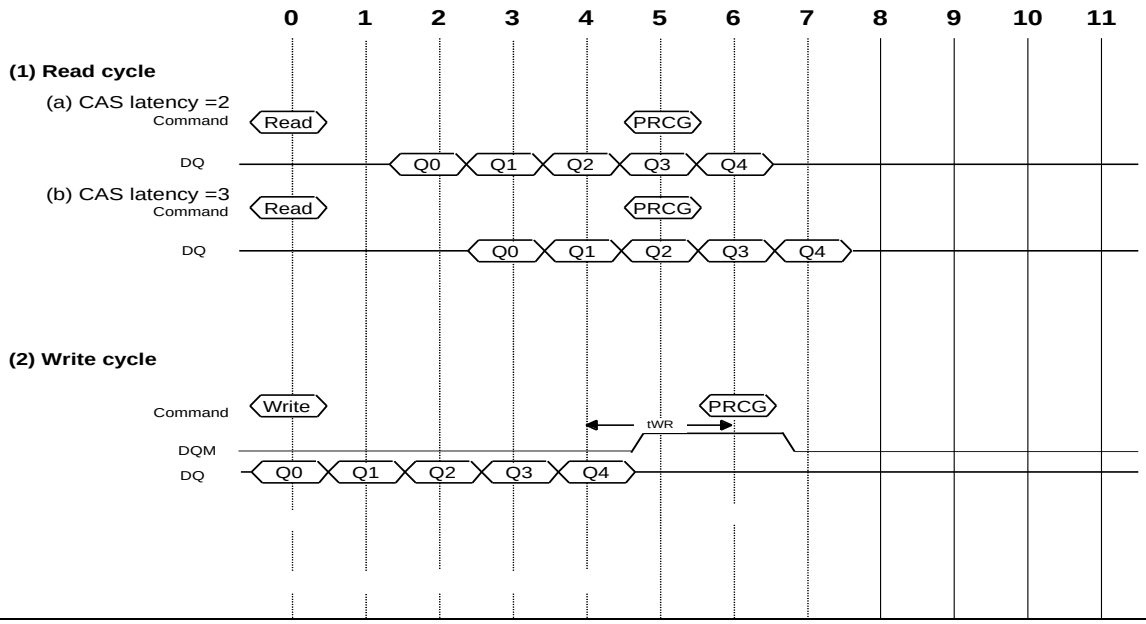


## 11.19 Timing Chart of Burst Stop Cycle (Burst Stop Command)

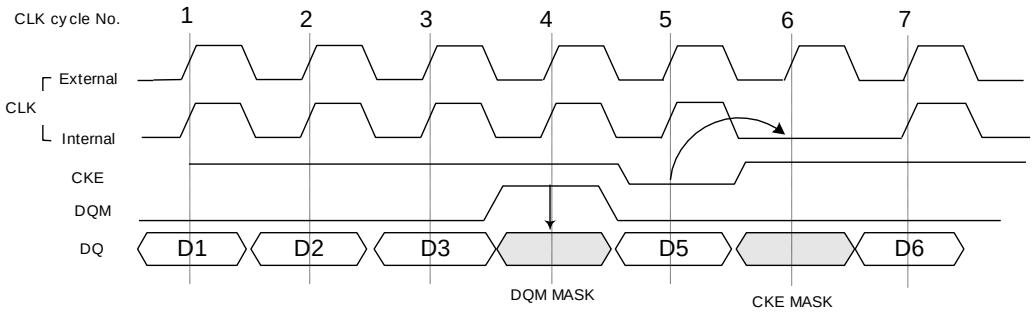



Note: BST represents the Burst stop command

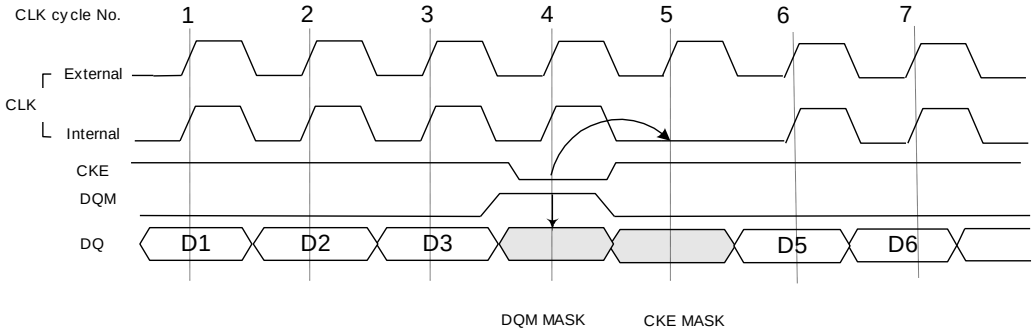
## 11.20 Timing Chart of Burst Stop Cycle (Precharge Command)



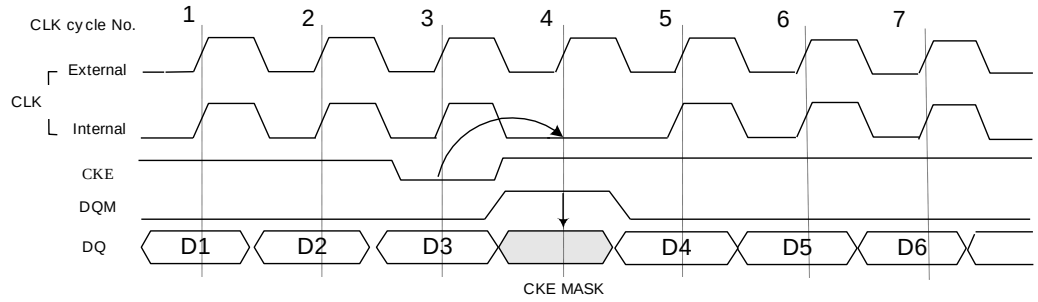
## 11.21 CKE/DQM Input Timing (Write Cycle)




( 1 )

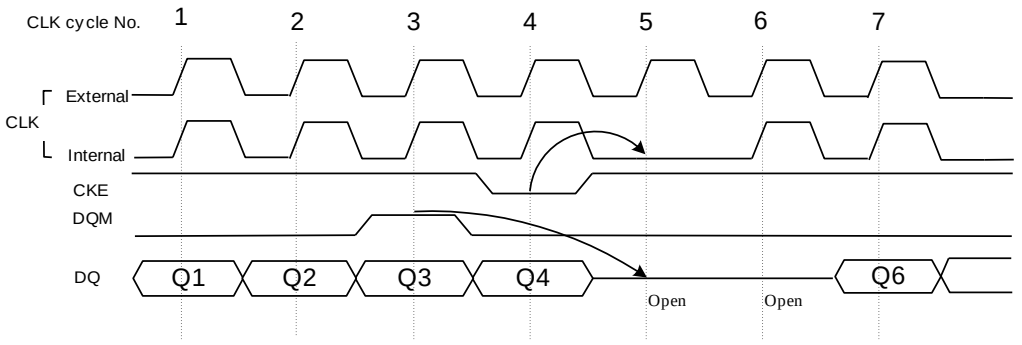



( 2 )

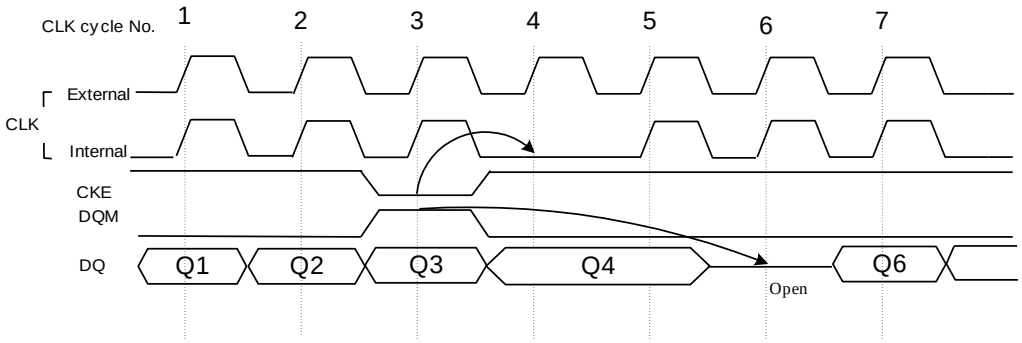



( 3 )

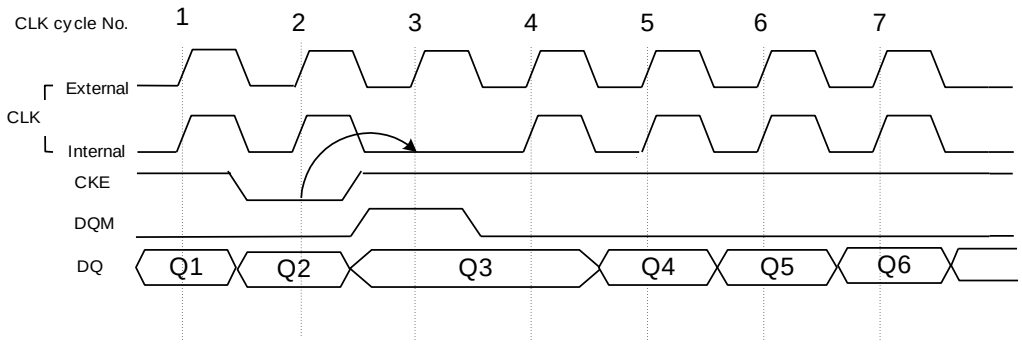
## 11.22 CKE/DQM Input Timing (Read Cycle)




( 1 )



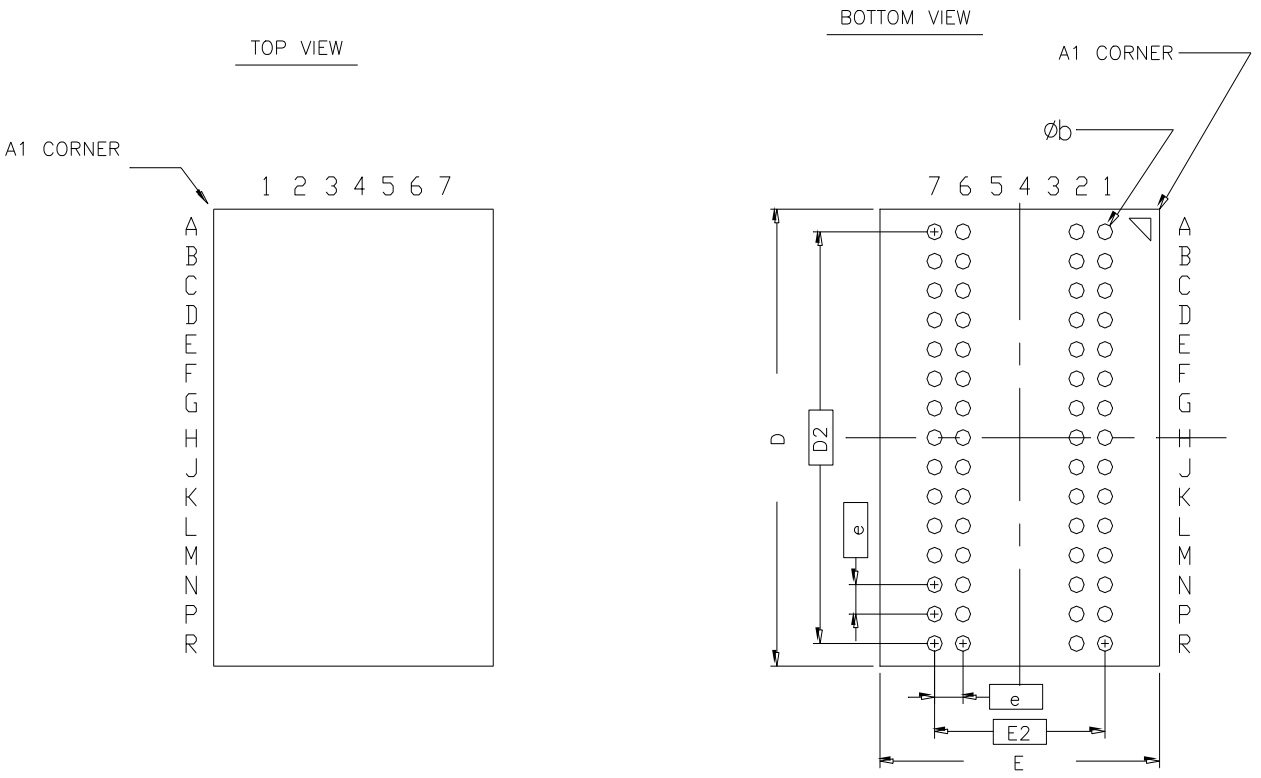

( 2 )




( 3 )

## 12. PACKAGE SPECIFICATION

### 12.1 VFBGA 60 Ball (6.4X10.10 mm, Ball pitch:0.65mm, Ø =0.4mm)




Controlling Dimension :Millimeters

| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | – | – | 1.10 | – | – | 0.0433 |
| A1 | 0.27 | – | 0.37 | 0.0106 | – | 0.0145 |
| D | 10.0 | 10.1 | 10.2 | 0.3937 | 0.3976 | 0.4015 |
| D2 | 9.10 REF. | | | 0.3582 REF. | | |
| E | 6.30 | 6.40 | 6.50 | 0.2480 | 0.2519 | 0.2559 |
| E2 | 3.90 REF. | | | 0.1535 REF. | | |
| y | 0.08 REF. | | | 0.0031 REF. | | |
| Øb | 0.35 | 0.4 | 0.45 | 0.0145 | 0.0157 | 0.0185 |
| e | --- | 0.65 | --- | --- | 0.0255 | --- |

Note: Ball Land: 0.45mm / Ball opening: 0.35mm

## 13. REVISION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---|---|---|---|
| A01 | Dec. 24, 2009 | All | Initial formal data sheet |
| A02 | Mar. 28, 2011 | 3, 13~16 | Add -6I industrial speed grade parts |


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